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# MS-7681

ATX(Full Size)  
Ver: 2.01

## CPU:

INTEL - Sandy Bridge LGA 1155

## System Chipset:

INTEL - Cougar Point PCH

## OnBoard Chipset:

Clock Gen:IDT 4106  
HD Audio Codec:RTL892  
LAN:RTL 8111E 10/100/1000 NIC X 2  
SIO:FIN71889AD  
ESATA Controller: JM363  
USB3.0: UPD720200F1  
Flash ROM: 64 Mb SPI (PCH)  
1394 Controller: VT6308P  
SATA 6G Marvel 9128

## Main Memory:

DDRIII (1066/1333MHz) \* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 2  
PCI Express (X1) Slot \* 3  
PCI Slot \* 2(From IDT TSI383)

## PWM:

CPU:UPI6234(5PHASE)  
CPU\_VTT:UP6113A(1PHASE)  
CPU\_SA:UP6113A (1PHASE)  
DDR/PCH PWR:UP6103A

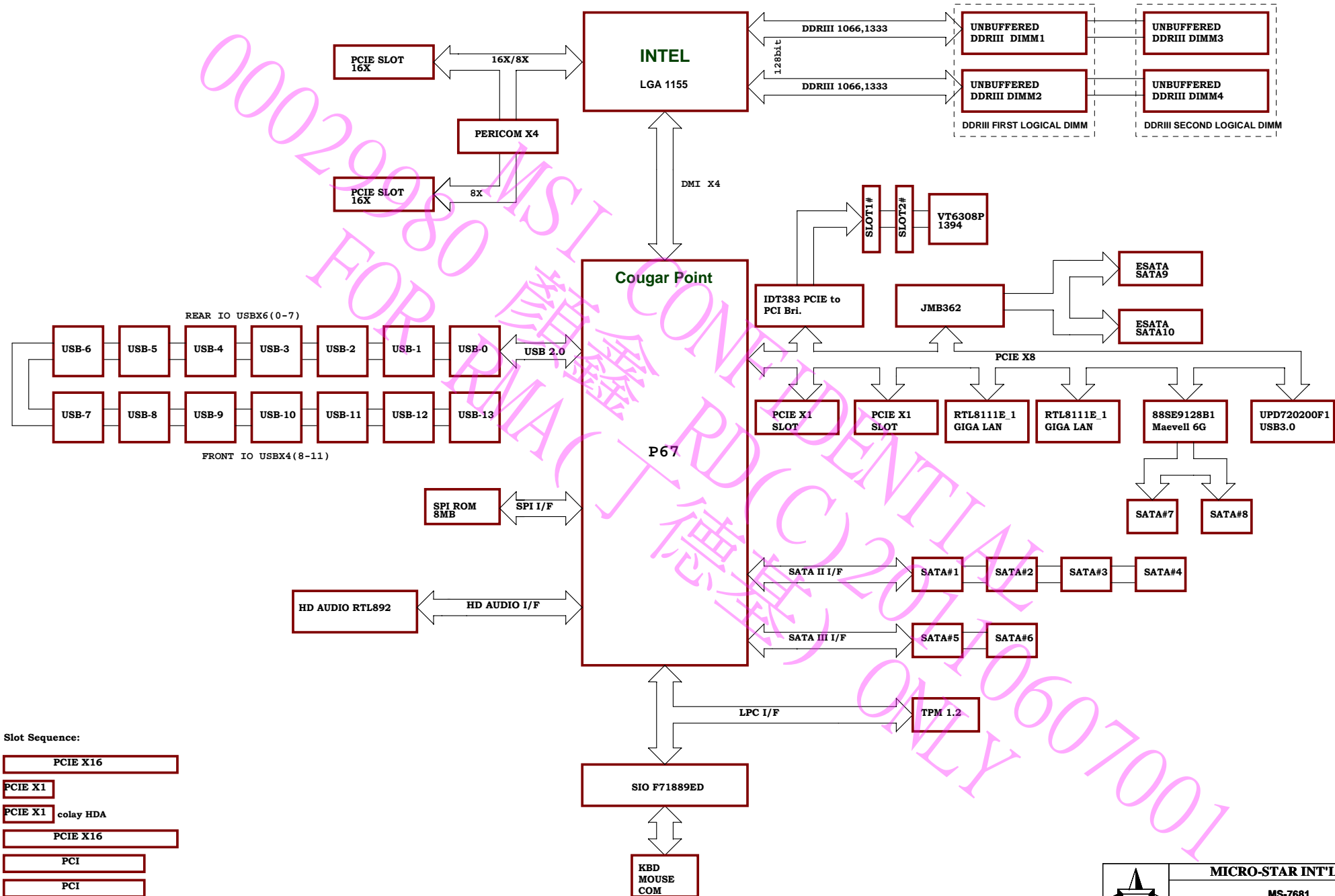
## Other:

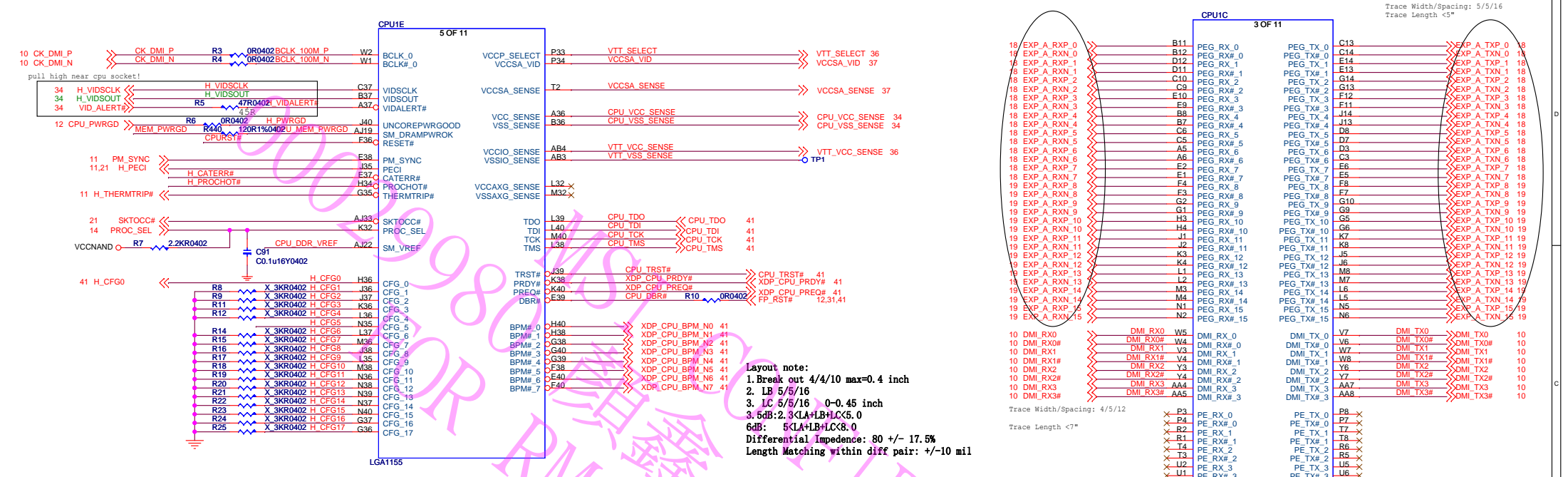
SATA3.0 x2+SATA2.0 x4 (PCH)  
ESATA2.0 x2 (JMB363)  
USB2.0 \*4 (Rear\*8 Front\*4)  
COM Header \*1  
USB3.0 \*4 (Rear\*2 Front\*2)

## ACPI:

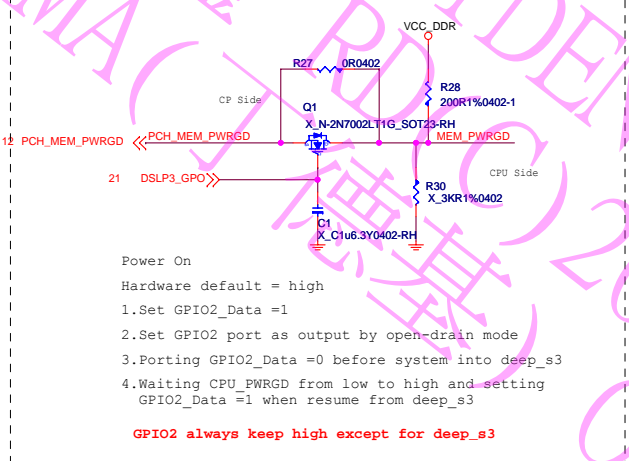
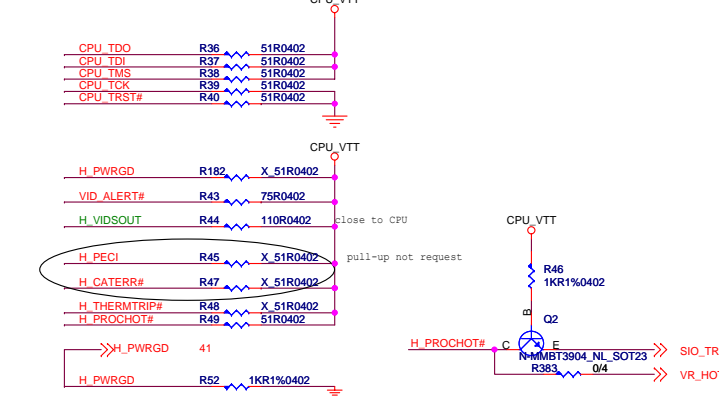
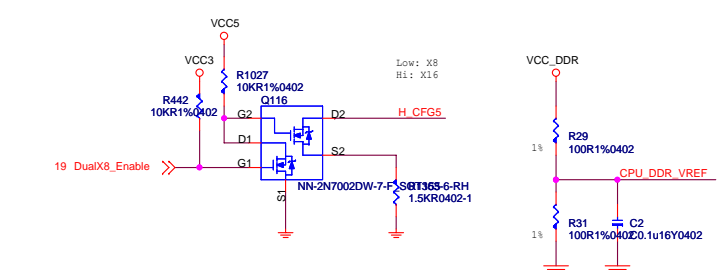
UPI



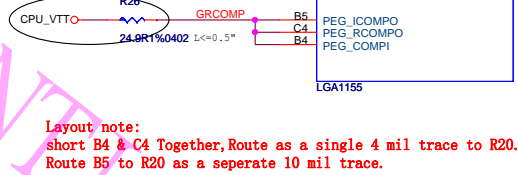




Layout note:  
1. Break out 4/4/10 max=0.4 inch  
2. LB 5/5/16  
3. LC 5/5/16 0-0.45 inch  
3.5dB: 2.3<LA+LB+LC<5.0  
6dB: 5<LA+LB+LC<8.0  
Differential Impedance: 80 +/- 17.5%  
Length Matching within diff pair: +/-10 mil



- Power On  
Hardware default = high
1. Set GPIO2\_Data = 1
  2. Set GPIO2 port as output by open-drain mode
  3. Porting GPIO2\_Data = 0 before system into deep\_s3
  4. Waiting CPU\_PWRGD from low to high and setting GPIO2\_Data = 1 when resume from deep\_s3
- GPIO2 always keep high except for deep\_s3



Layout note:  
short B4 & C4 Together, Route as a single 4 mil trace to R20.  
Route B5 to R20 as a separate 10 mil trace.

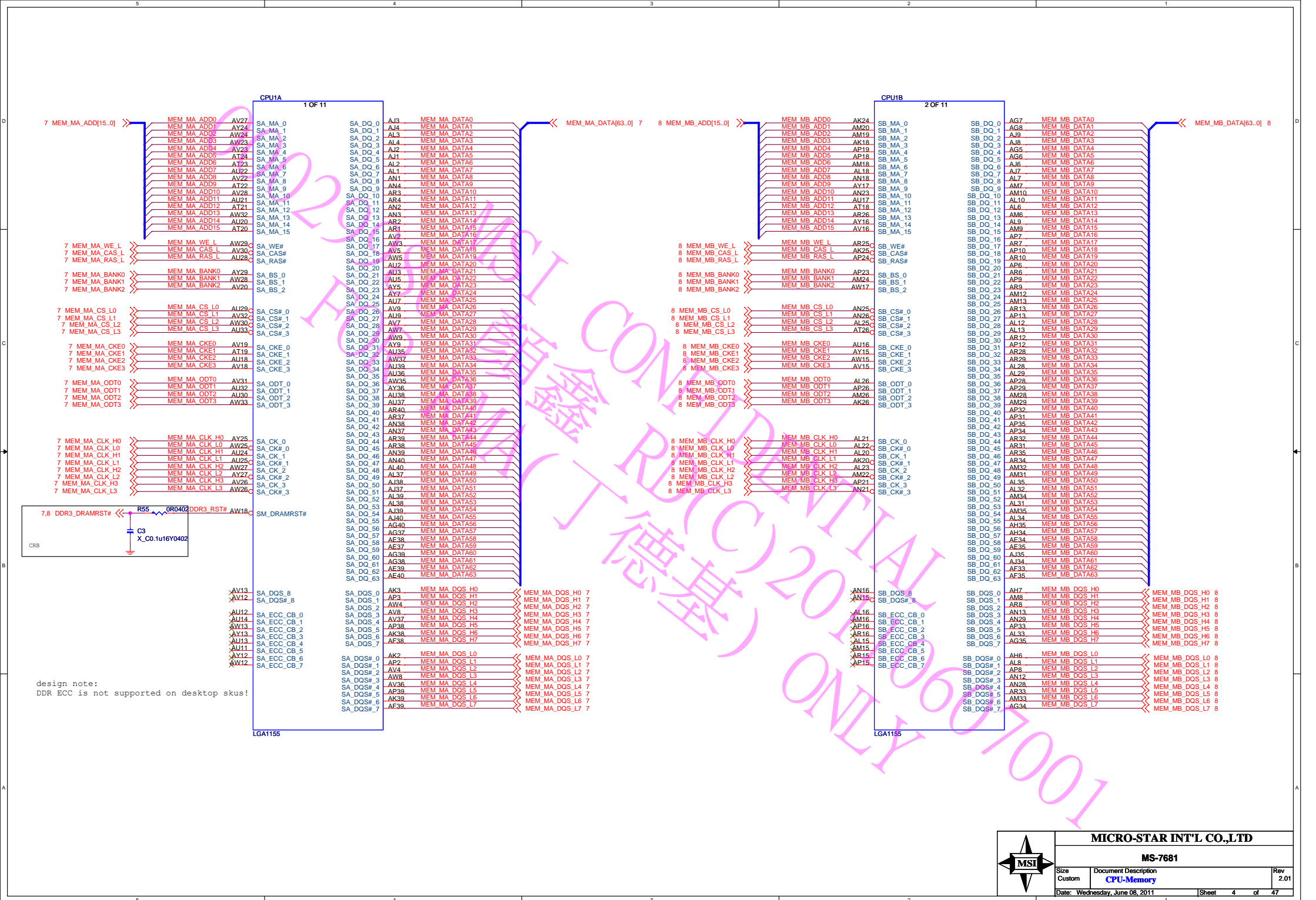
PEG CONFIG TABLE			
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

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**MS-7681**

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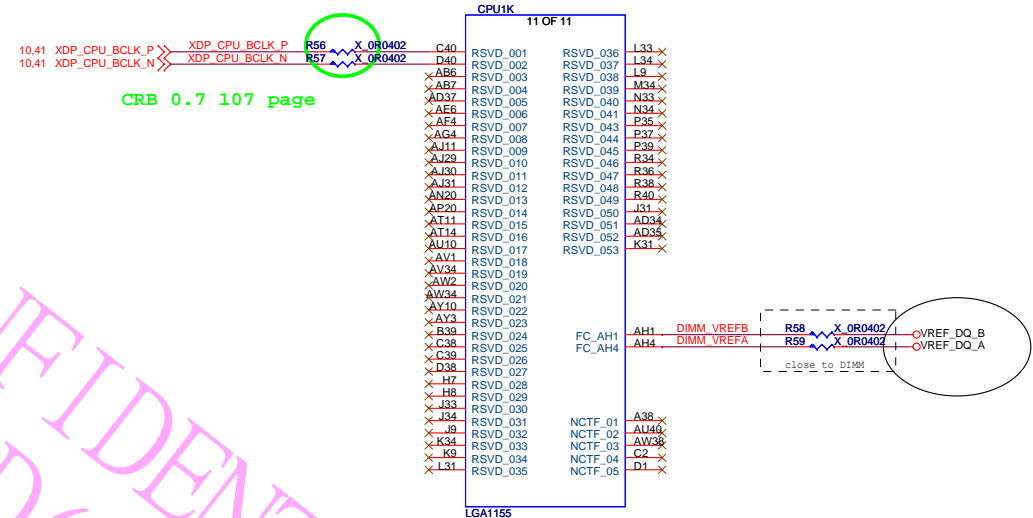
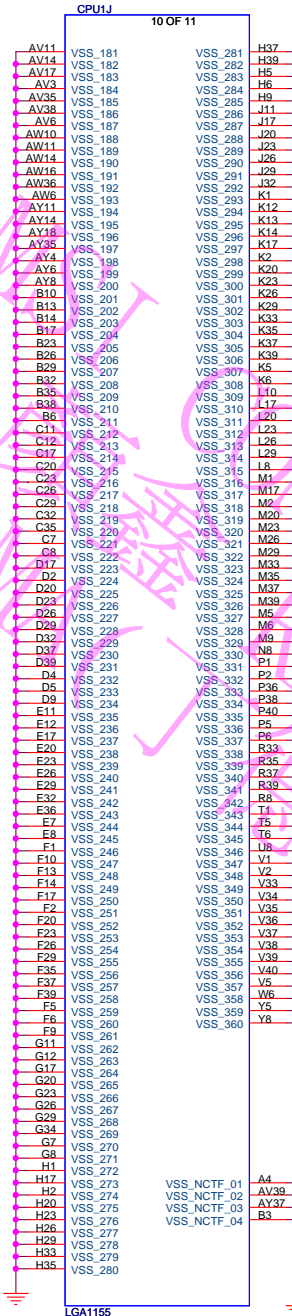
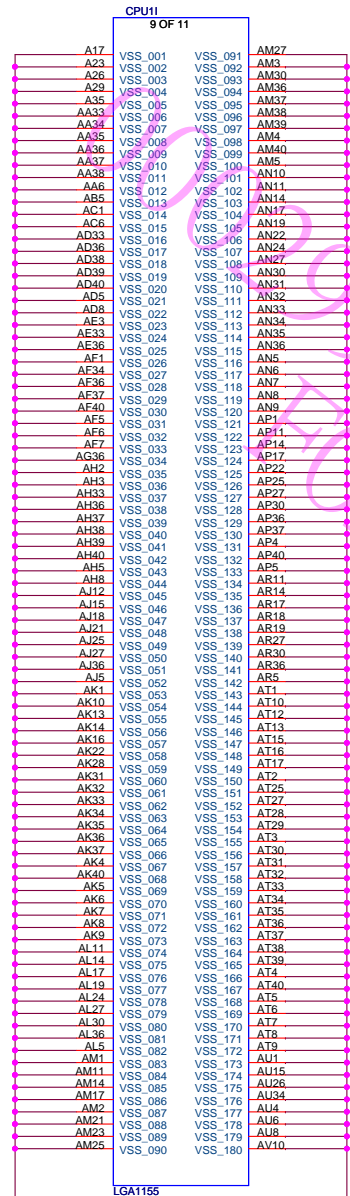
**MICRO-STAR INT'L CO.,LTD**

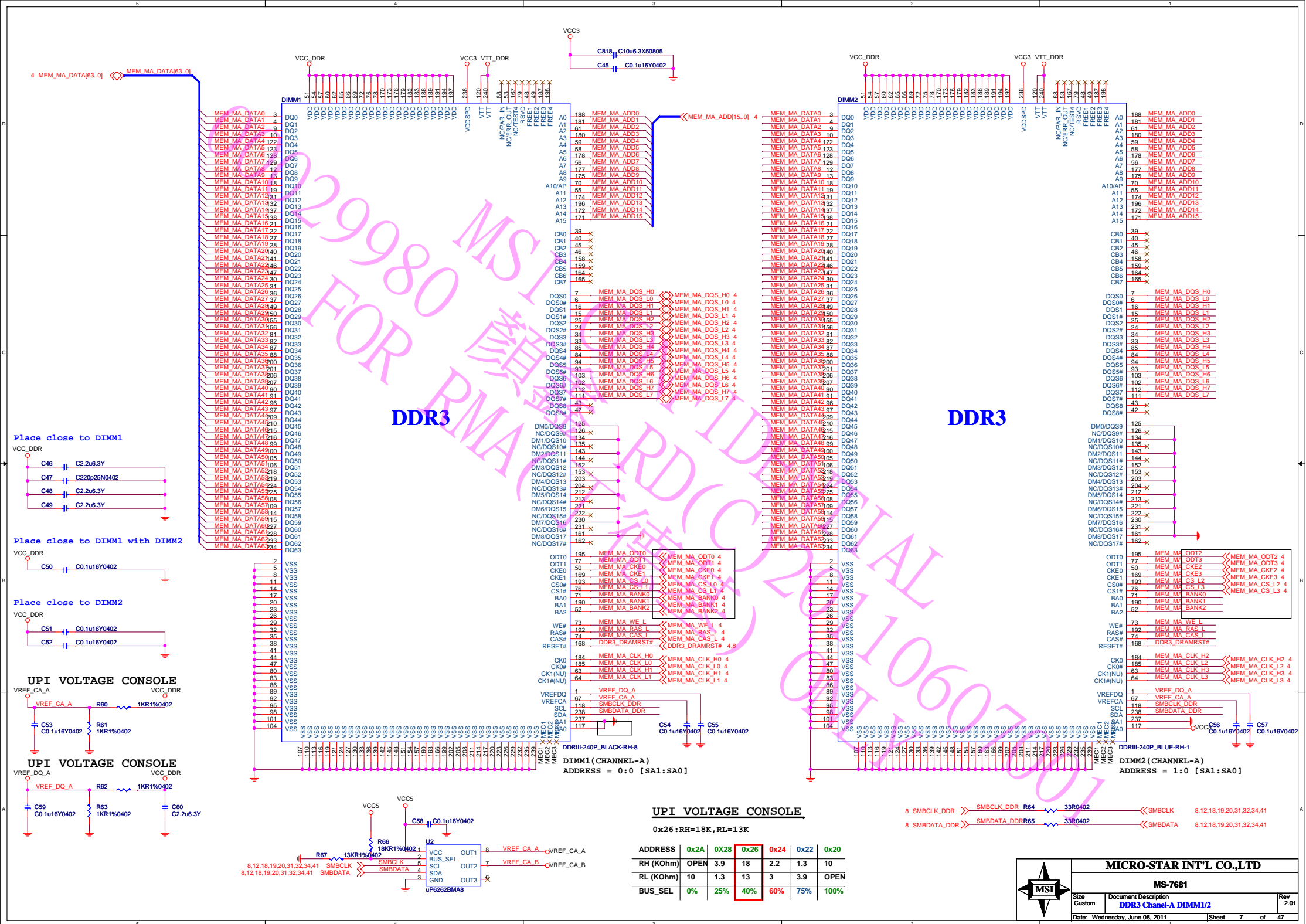
MS-7681

Size Custom	Document Description <b>CPU-Memory</b>	Rev 2.01
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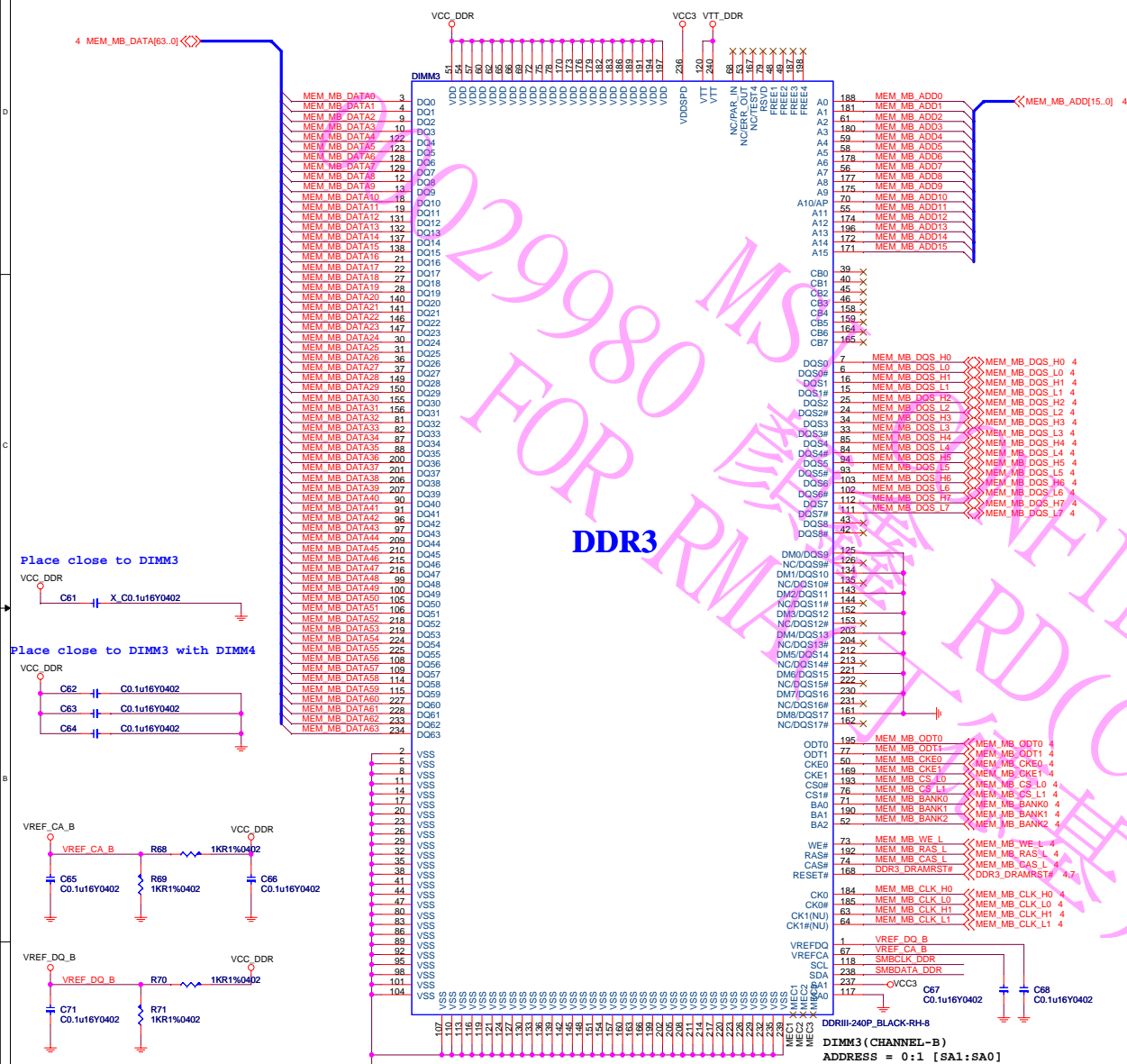




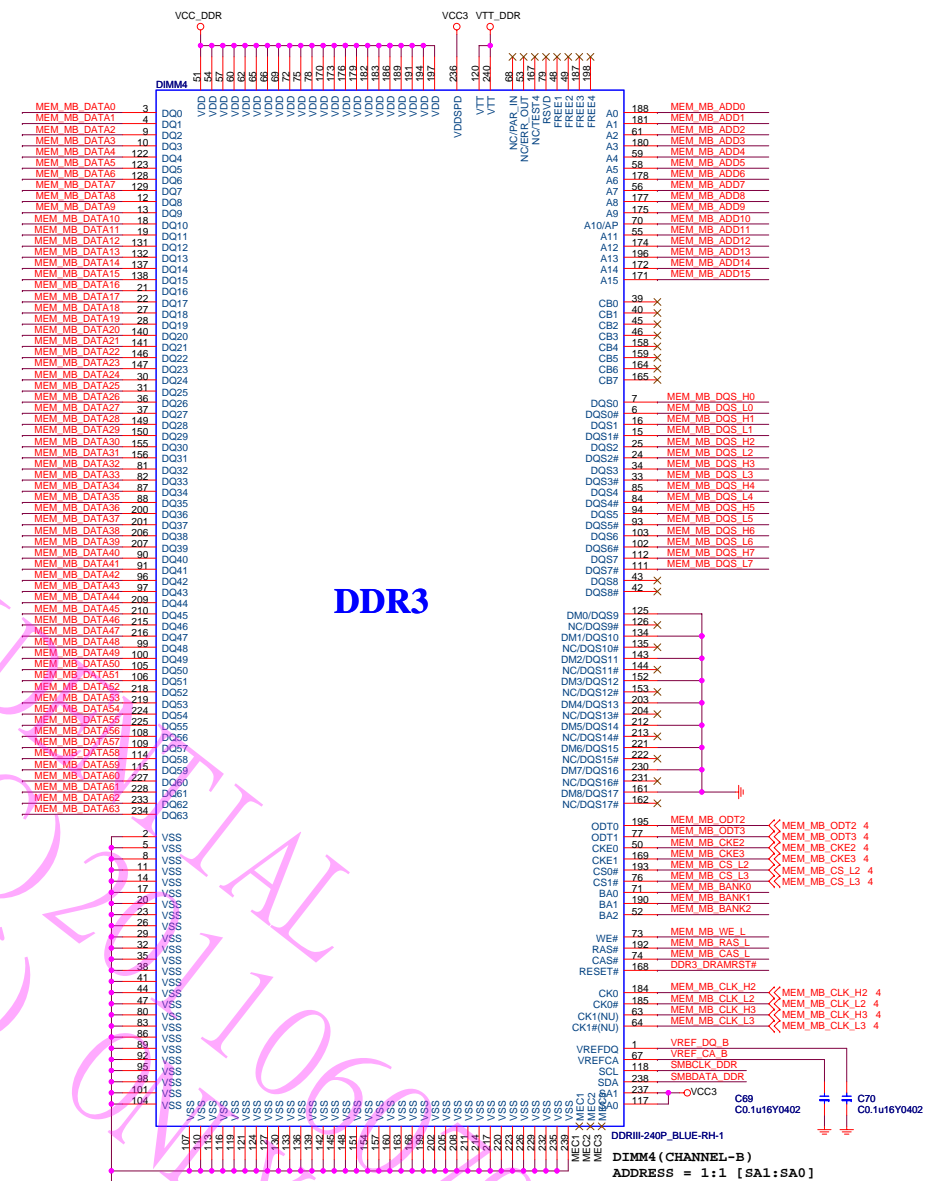




## DDRIII DIMM\_B0



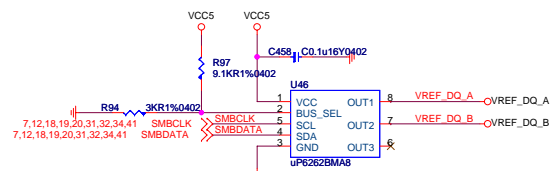
## DDRIII DIMM\_B1



UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	9.1	3	2.2	1.3	10
RL (KOhm)	10	3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



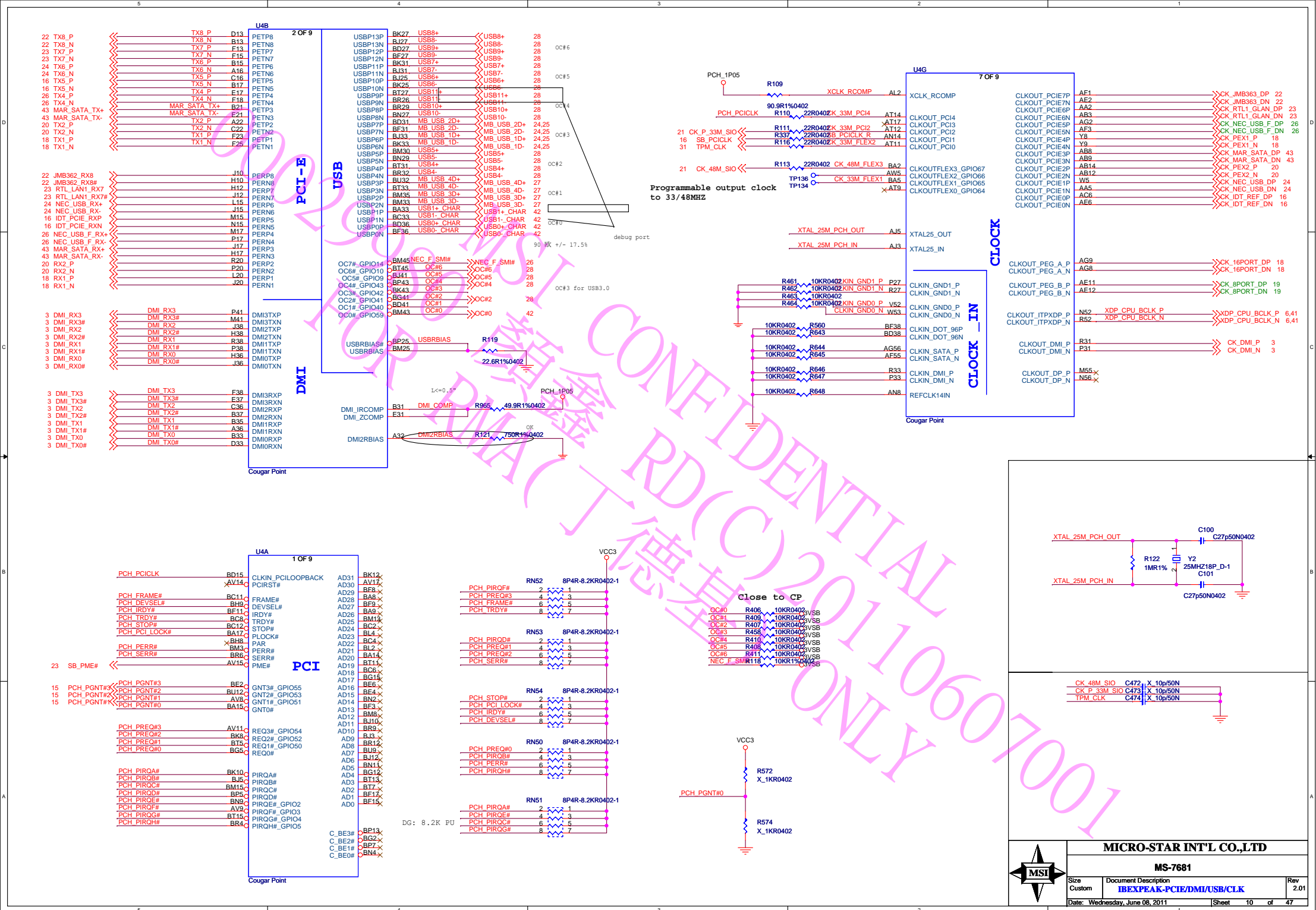
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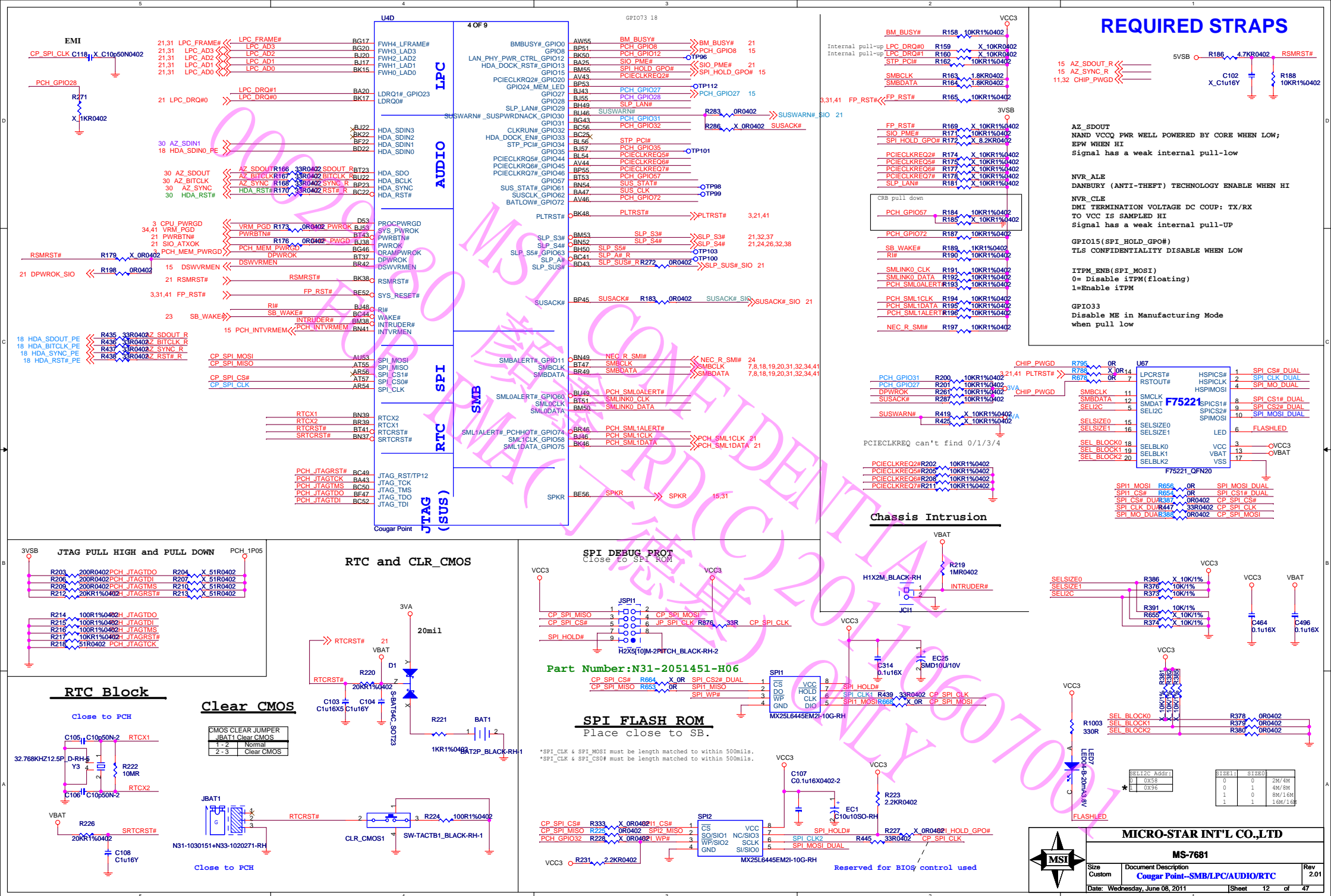
Size Custom	Document Description <b>DDR3 Chanel-B DIMM3/4</b>	Rev 2.0
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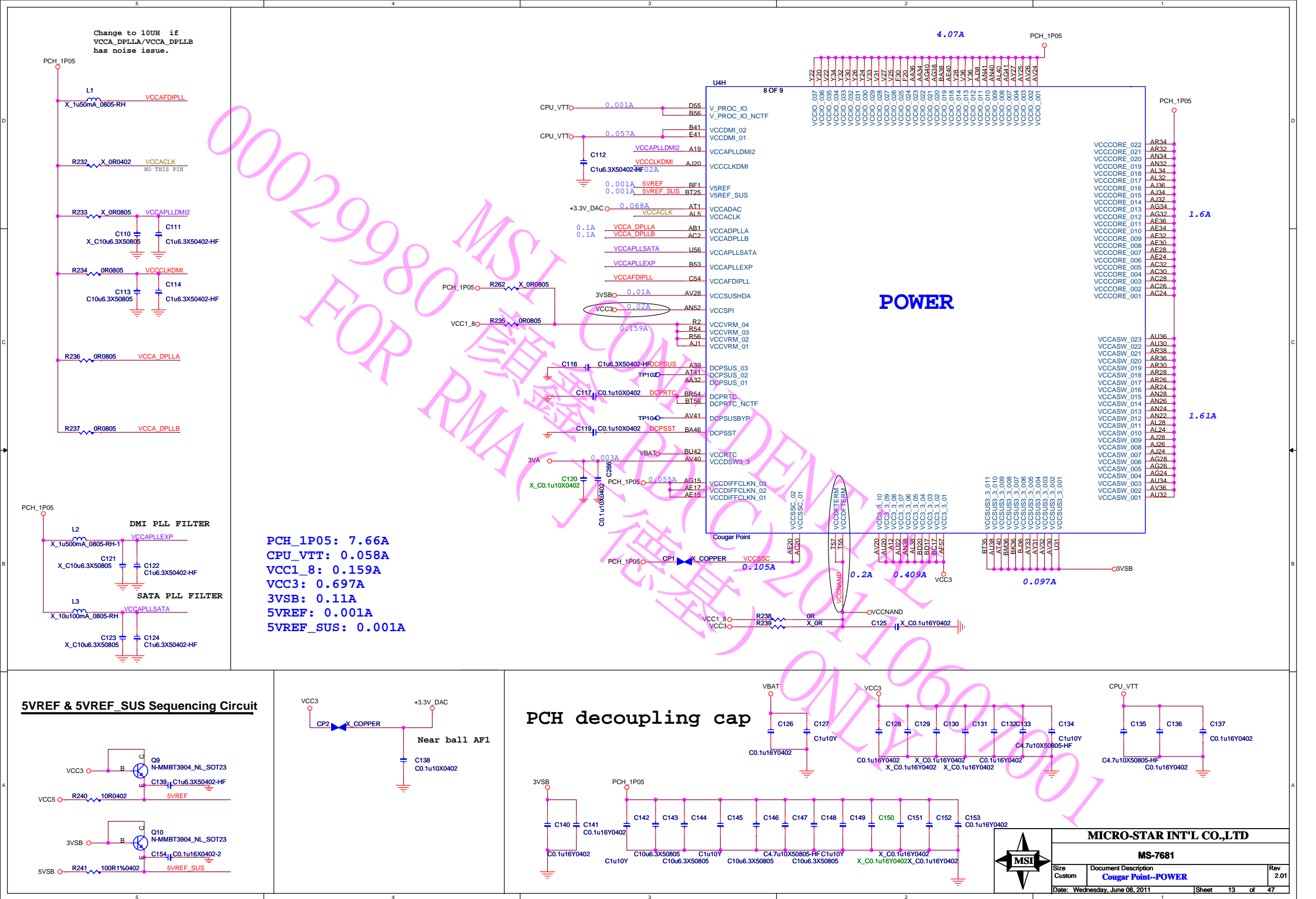


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FOR RMA(顏金鑫 RD(C)20110607001)  
(丁德基) ONLY







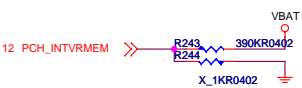
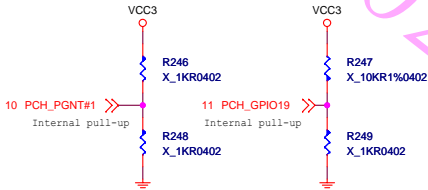




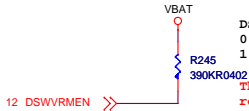


PCH Straps

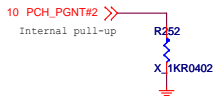
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



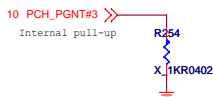
INTVRMEN  
0: DISABLE INTERNAL VRM  
1: ENABLE INTERNAL VRM \*  
  
When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



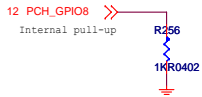
DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.  
  
This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



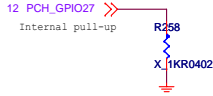
DIM AC/DC MODE  
0 : AC  
1 : DC \*



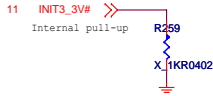
Topblock swap override when pull-low  
Signal has a weak internal pull-up



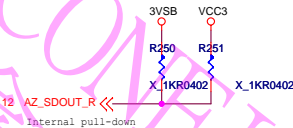
GPIO8  
0 : Integrated Clocking Enable (FCIM)\*  
1 : Buffer Through Mode Enable (BTM)



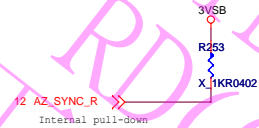
GPIO27  
0 : OD PLL VR disabled  
1 : OD PLL VR enabled \*  
Signal has a weak internal pull-up



INT3\_3V#  
0 : INIT3\_3V to asserted for 16 PCI clock to reset theprocessor by some evens occur  
1 : Can not to reset the processor



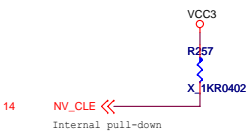
HDA\_SDO  
Disable ME in Manufacturing Mode  
when pull LOW ????



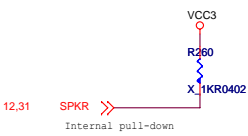
HDA\_SYNC  
OD PLL VR SUPPLY SEL  
0: 1.8V SUPPLY \*  
1: 1.5V SUPPLY



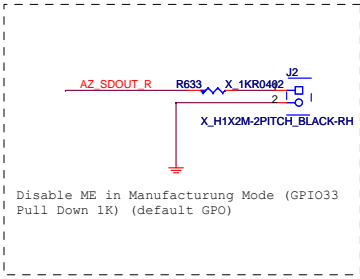
GPIO15  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



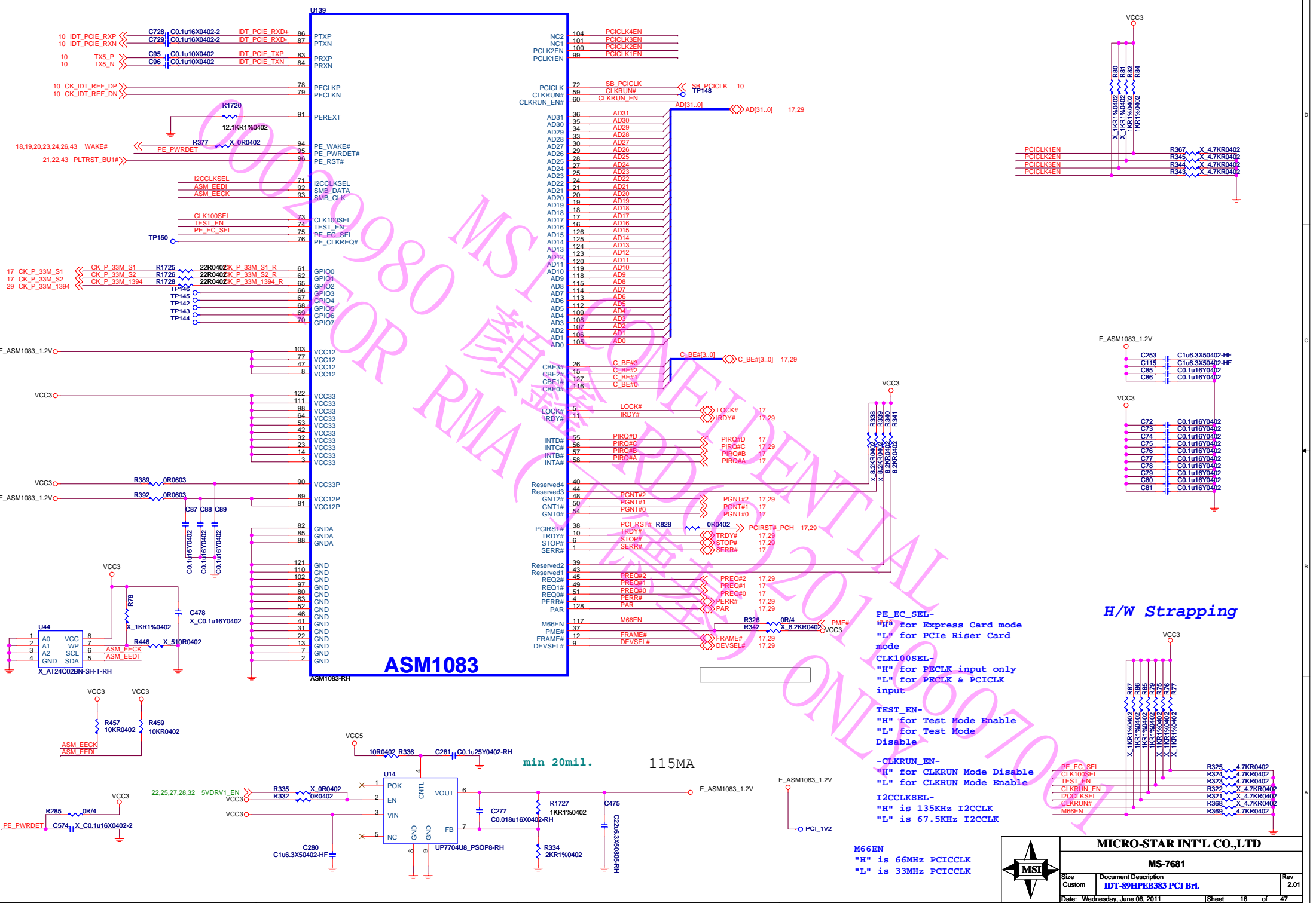
DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*?  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT

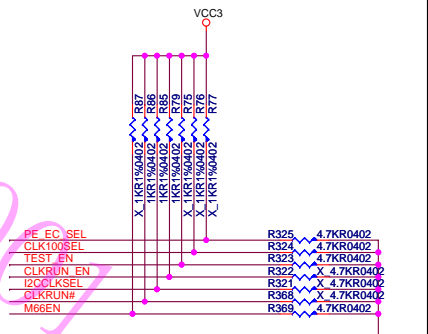


Disable ME in Manufacturing Mode (GPIO33)  
Pull Down 1K) (default GPO)



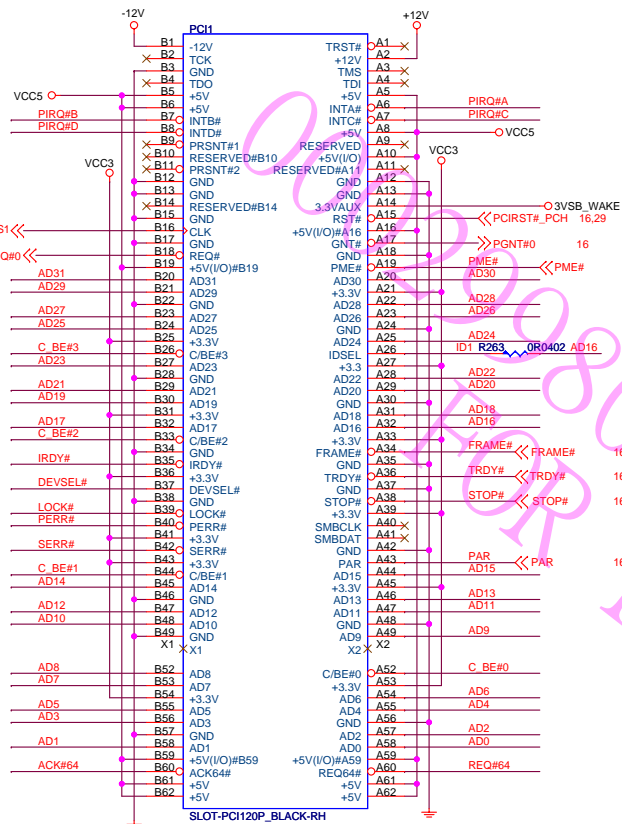
PE\_EC\_SEL-  
"H" for Express Card mode  
"L" for PCIe Riser Card mode  
CLK100SEL-  
"H" for PECLK input only  
"L" for PECLK & PCICLK input  
TEST\_EN-  
"H" for Test Mode Enable  
"L" for Test Mode Disable  
-CLKRUN\_EN-  
"H" for CLKRUN Mode Disable  
"L" for CLKRUN Mode Enable  
I2CCLKSEL-  
"H" is 135KHz I2CCLK  
"L" is 67.5KHz I2CCLK

### H/W Strapping



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MS-7681			
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**PCI SLOT 1 (PCI VER: 2.2 COMPLY)**



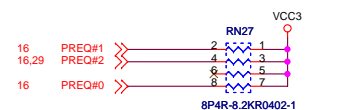
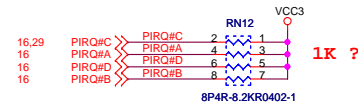
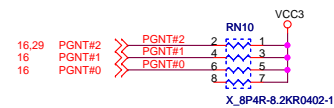
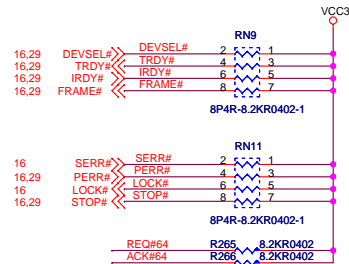
```

IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

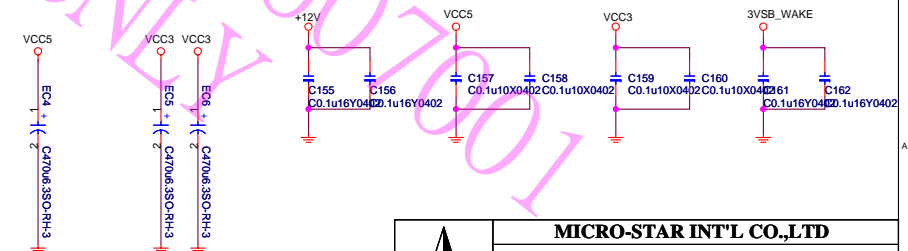
```



## PCI PULL-UP / DOWN RESISTORS



## PCI SLOT DECOUPLING CAPACITORS



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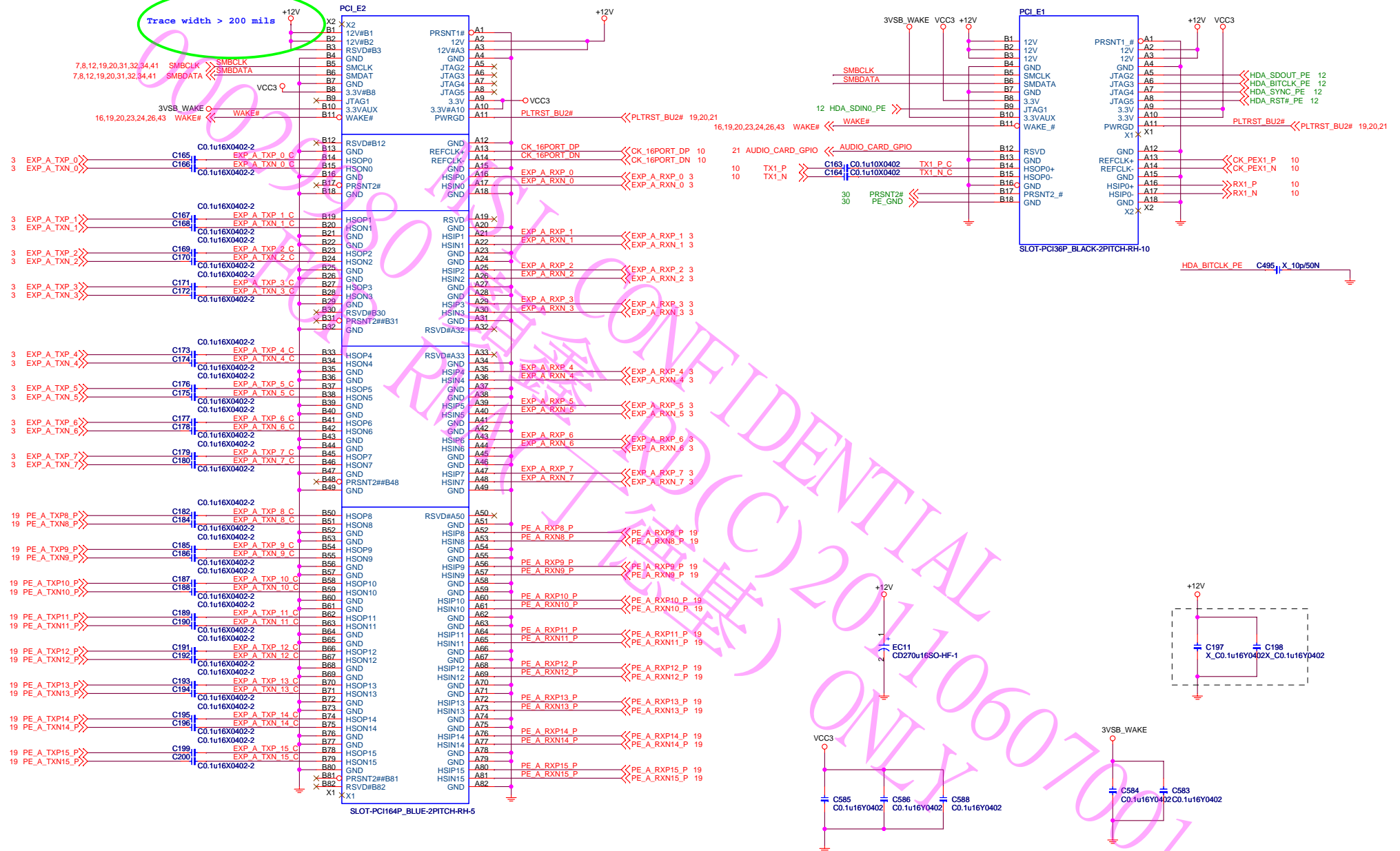
Size	Document Description	Rev
Custom	PCI Slot 1 & 2 & 3	2.01

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# PCI\_Express X16 Slot

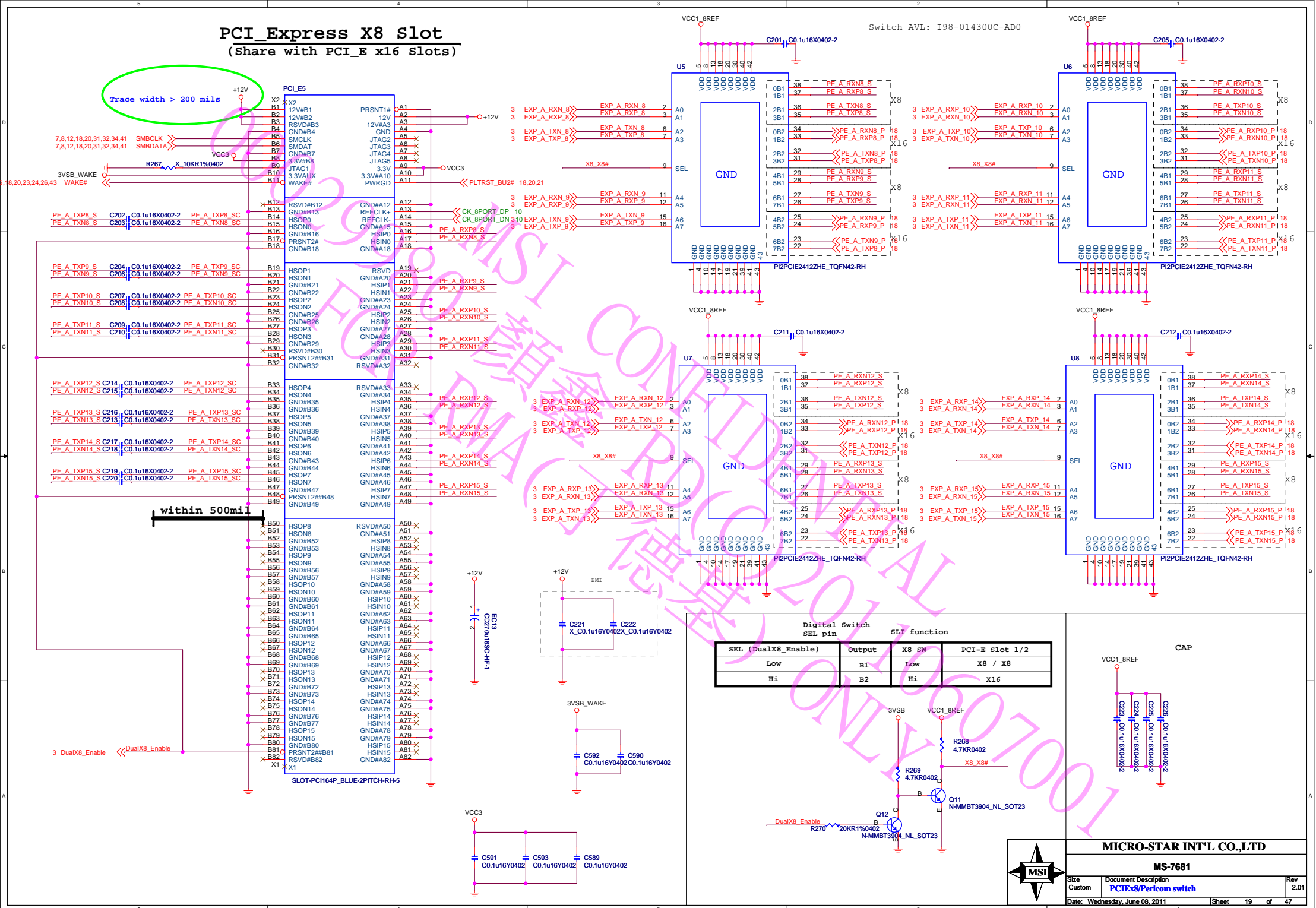
# HDA co-lay PCIe x1

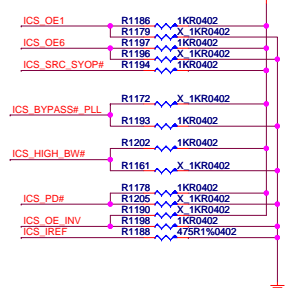
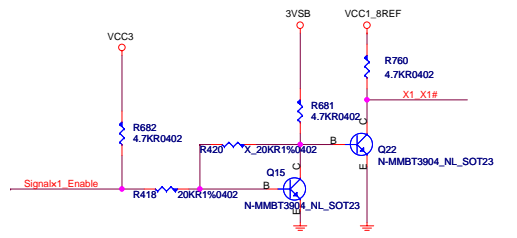
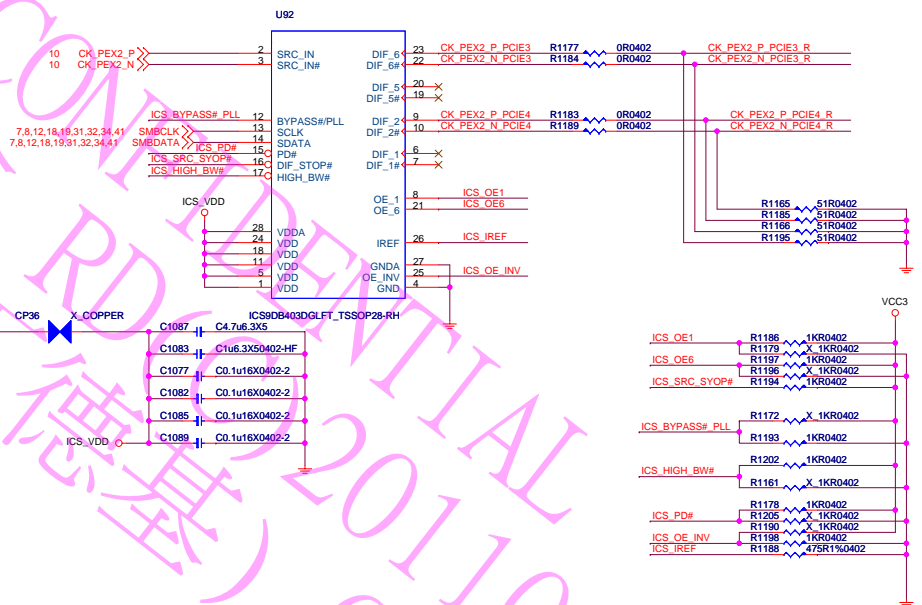
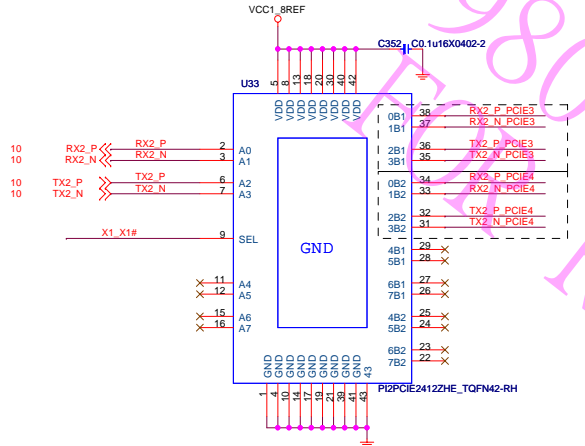
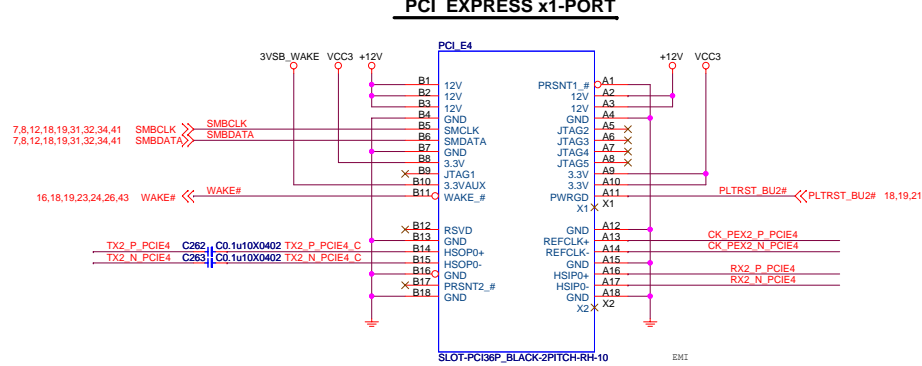
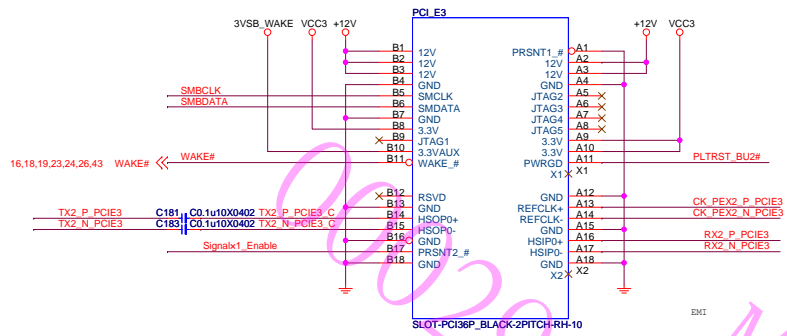
## PCI EXPRESS x1-PORT

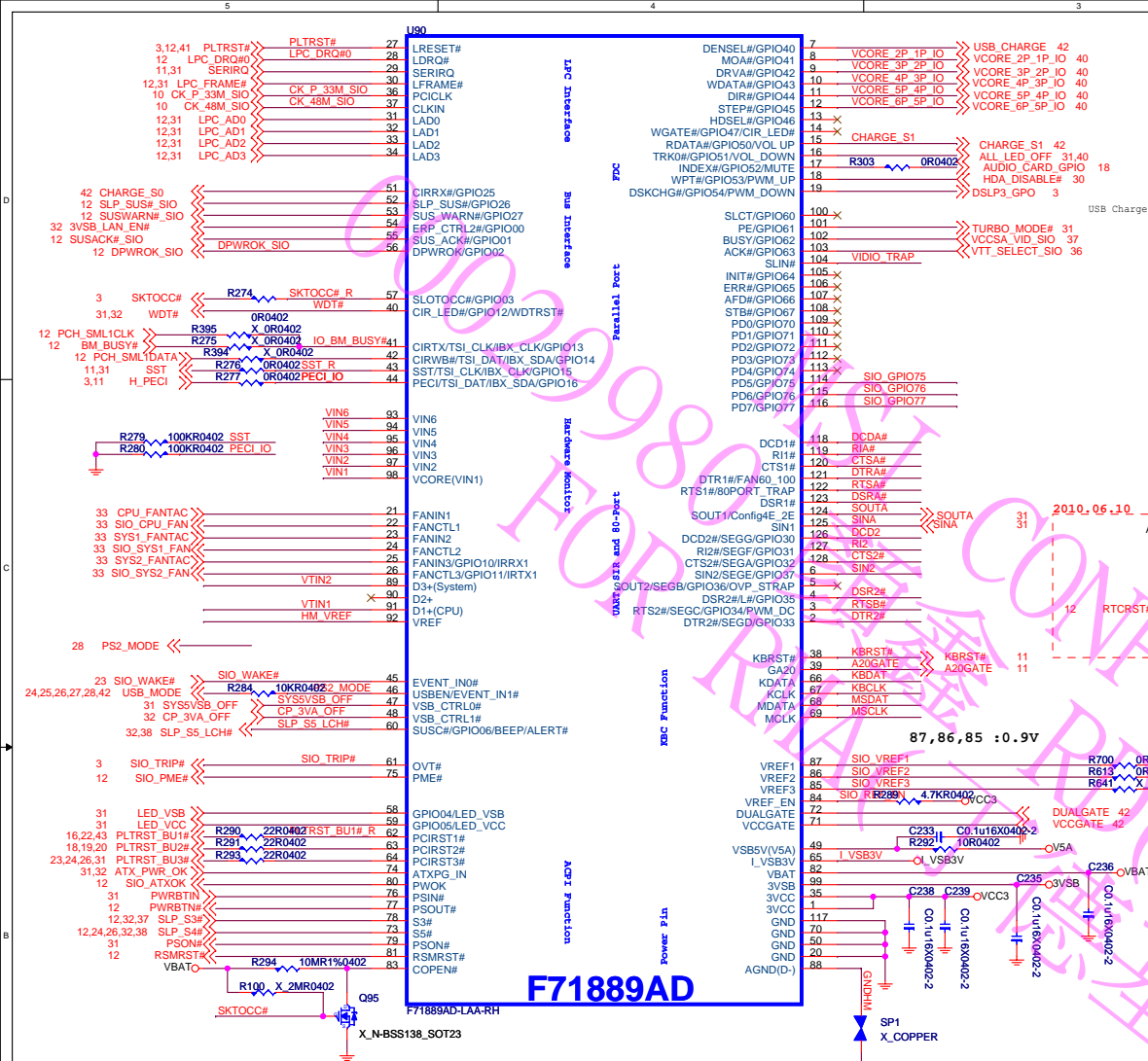




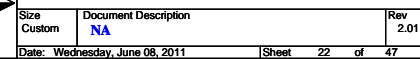
# PCI\_Express X8 slot (Share with PCI\_E x16 Slots)





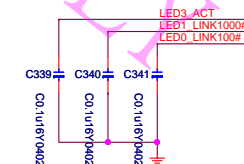
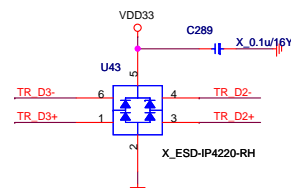
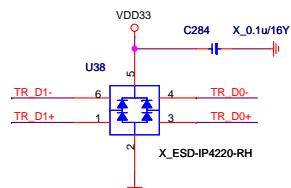
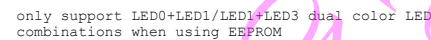
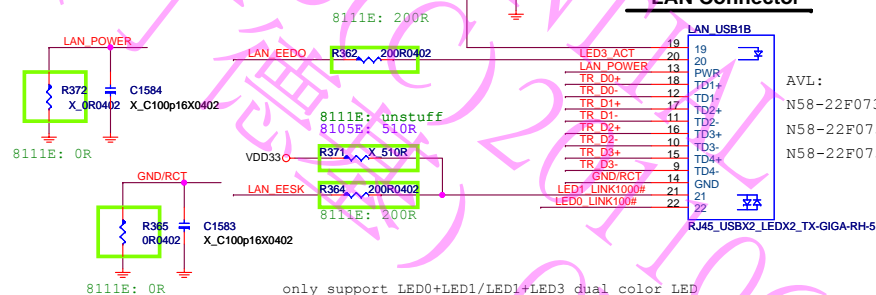
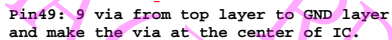
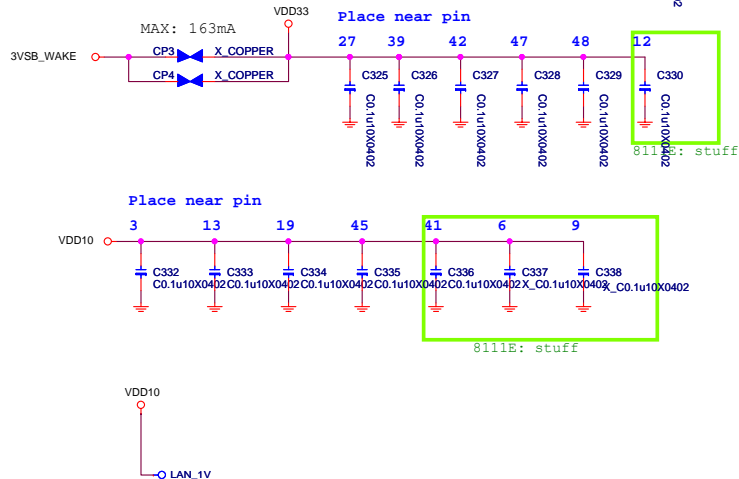
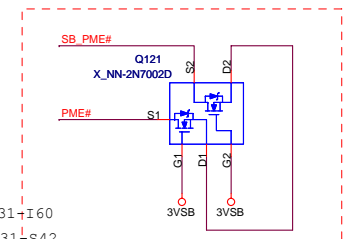
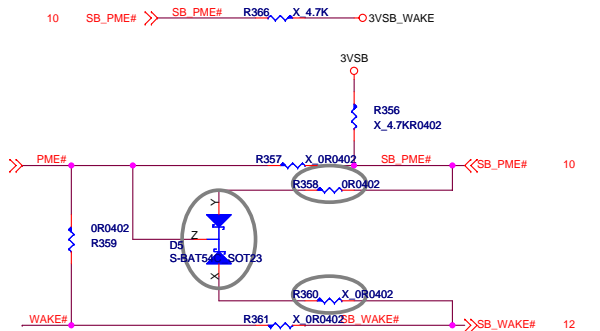
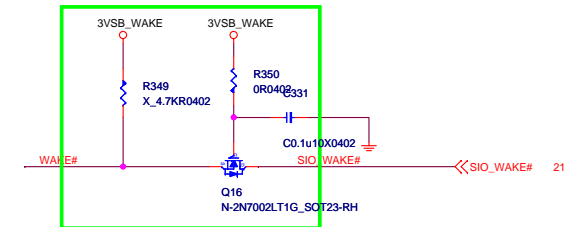
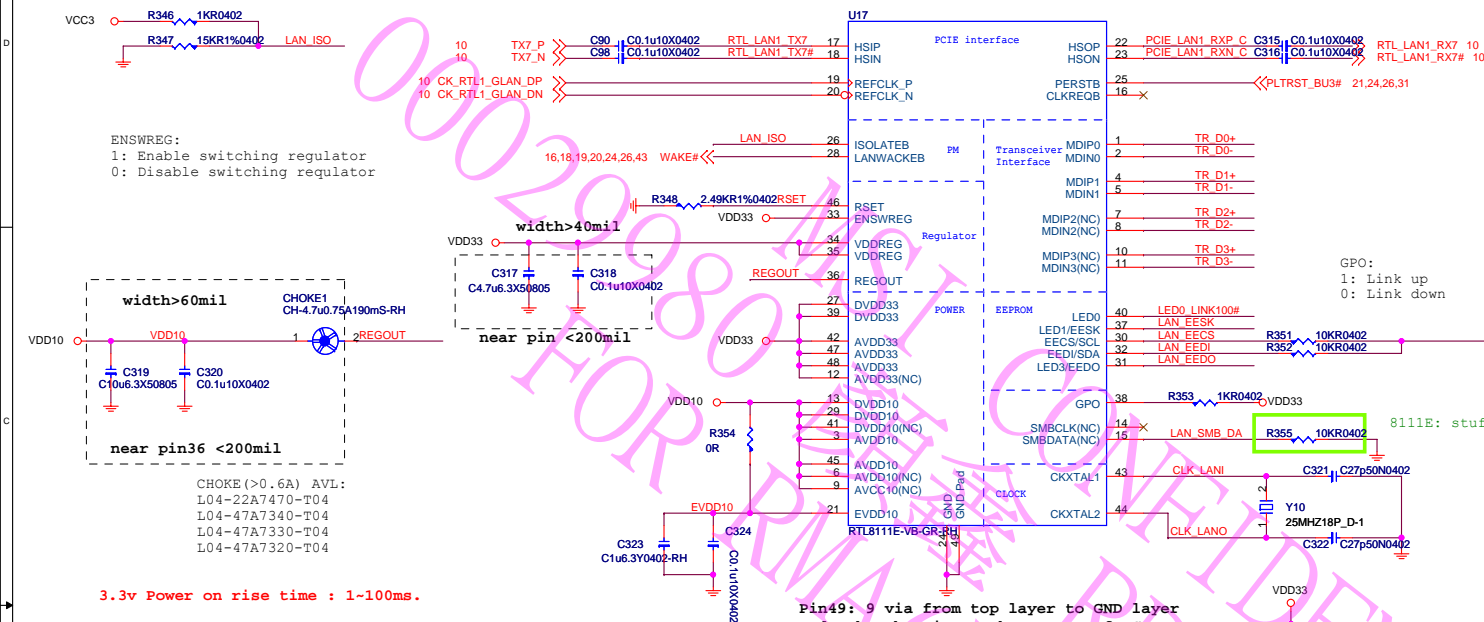


Pin4 and Pin9 over 20mil  
1/7/10 update.











# RTL8111E Giga LAN

### LAN/PCIE/PCI Wake Up CTRL Circuit



## 8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

Giga-Lan		10/100-Lan	
<b>N58-22F0731</b>		<b>N58-22F0771</b>	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	 Yellow	20	 Yellow
	Orange		
21		21	
22	 Green	22	 Green



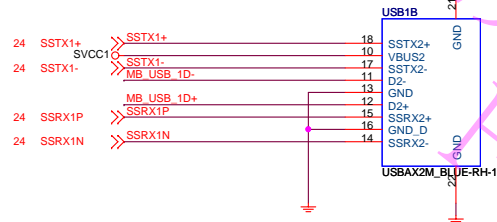
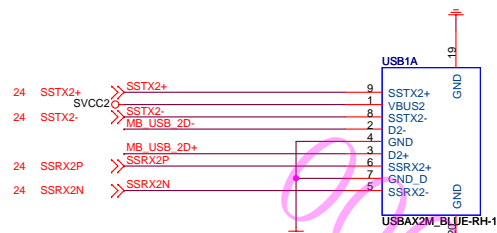
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**MS-7681**

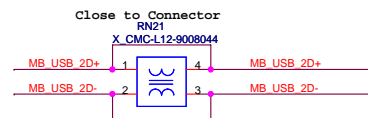
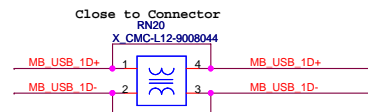
Size Custom	Document Description <b>LAN-RTL8111E-1</b>	Rev 2.01
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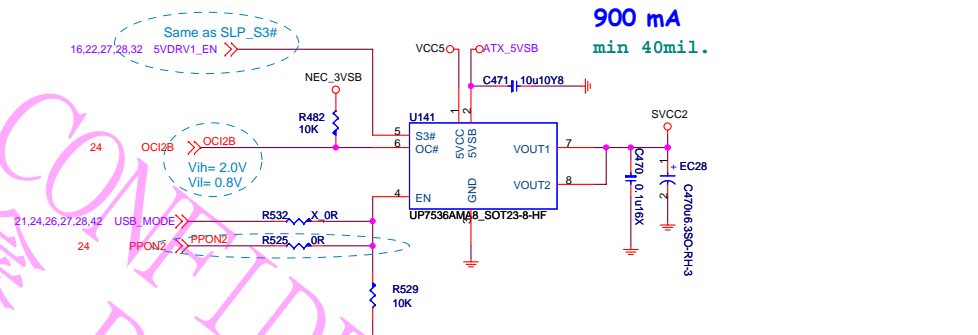
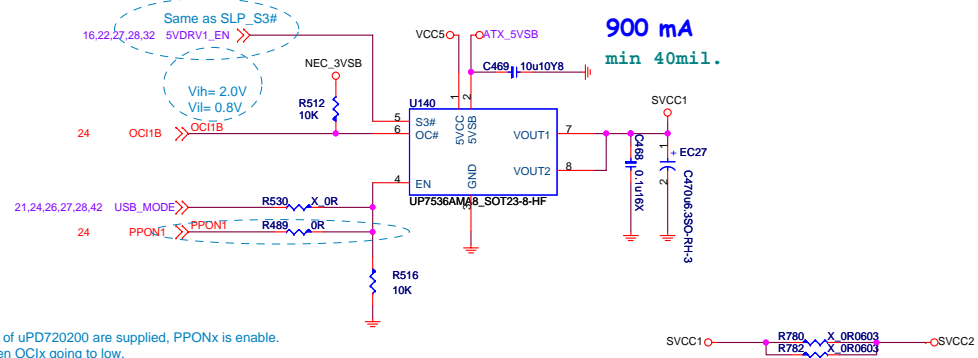




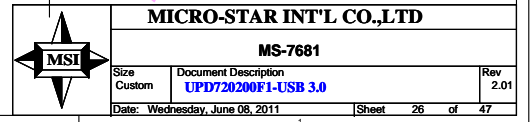
10,24 MB\_USB\_1D+ >>>  
 10,24 MB\_USB\_1D- >>>  
 10,24 MB\_USB\_2D+ >>>  
 10,24 MB\_USB\_2D- >>>

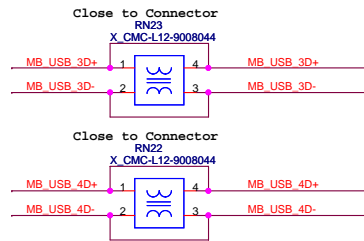
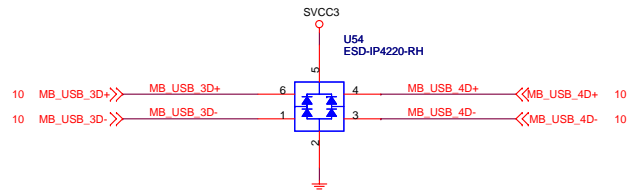
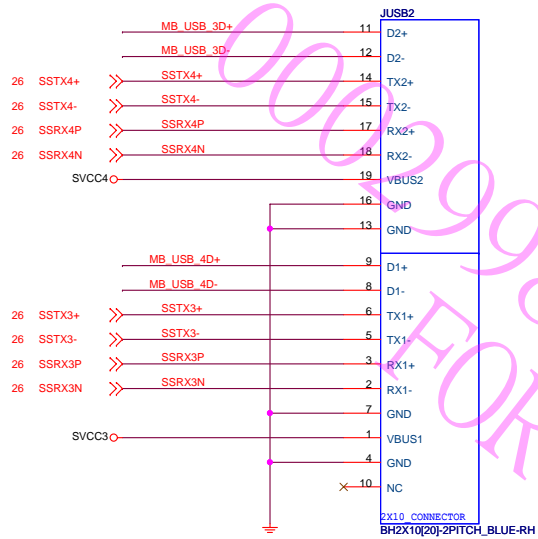


All power sources of uPD720200 are supplied, PPN0x is enable.  
 PPN0x is low when OC1x going to low.

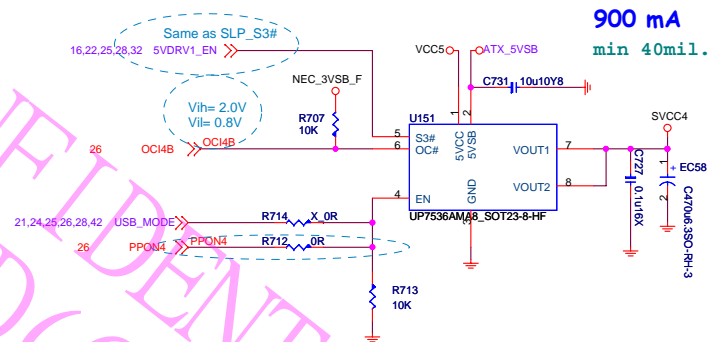
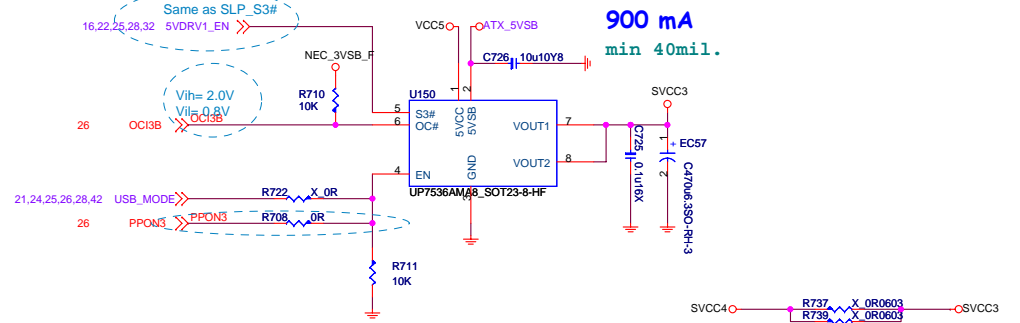


MICRO-STAR INT'L CO.,LTD			
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Custom	USB 3.0 Power & Connector		2.01
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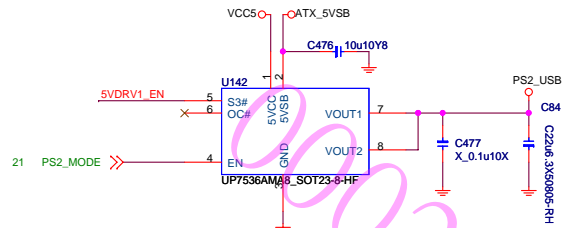


All power sources of uPD720200 are supplied, PPN0x is enable.  
PPN0x is low when OC1x going to low.



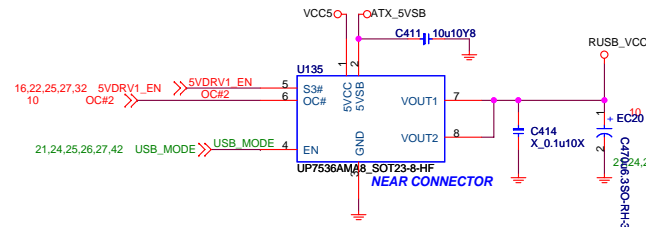
## Front USB Connector

### USB POWER FOR PORT 11,12

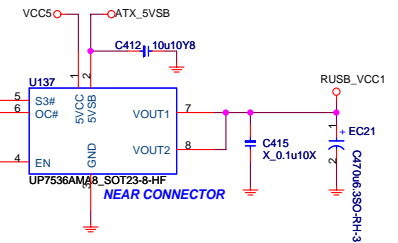


## Rear USB Connector

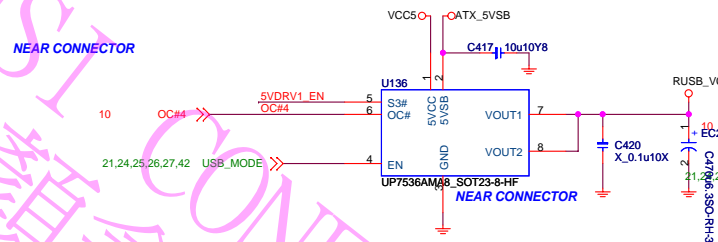
### USB POWER FOR PORT 4,5



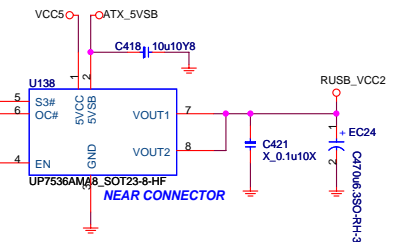
### USB POWER FOR PORT 6,7



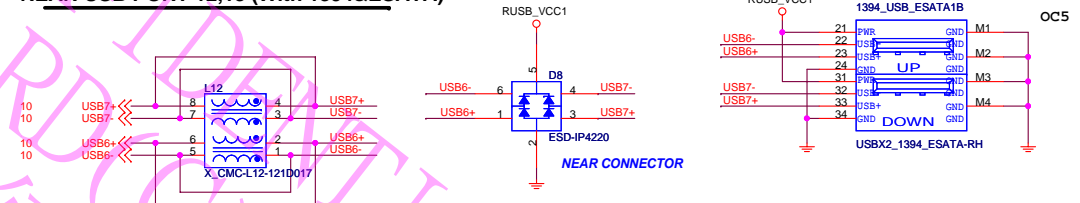
### USB POWER FOR PORT 11,12



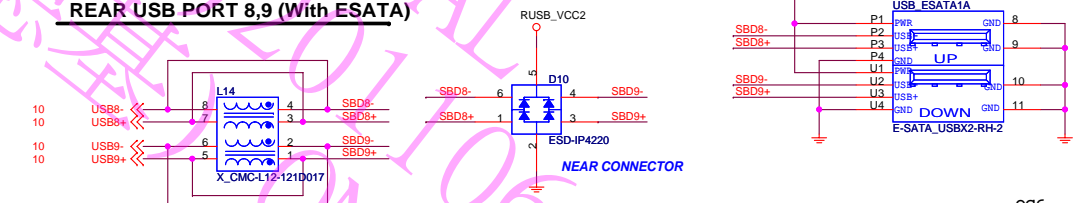
### USB POWER FOR PORT 8,9



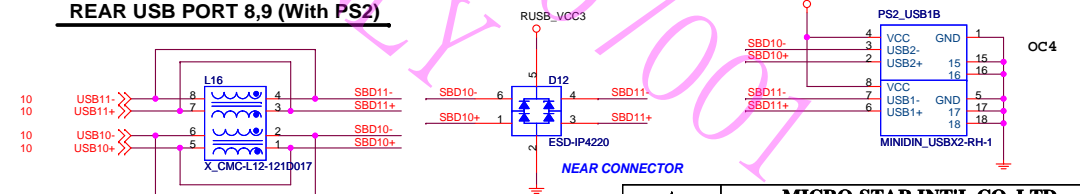
### REAR USB PORT 12,13 (With 1394&ESATA)



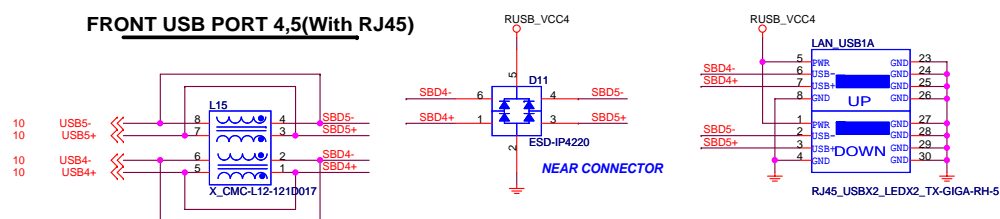
### REAR USB PORT 8,9 (With ESATA)



### REAR USB PORT 8,9 (With PS2)



### FRONT USB PORT 4,5(With RJ45)



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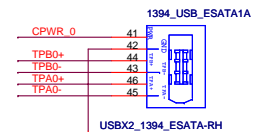
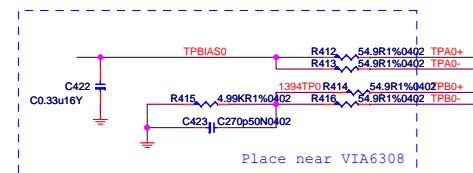
## **VT6308P - 1394 Controller**

Trace Width/Spceing: 4/10/4

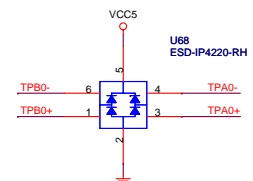
Impedance: 110  $\Omega$  / +/- 6

Trace Length: < 6"

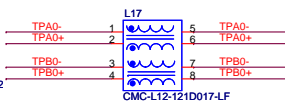
Rear 1394 port



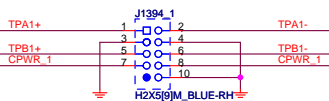
USBX2\_1394\_ESATA-RH



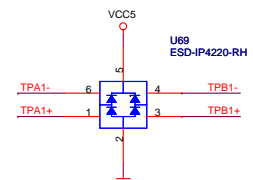
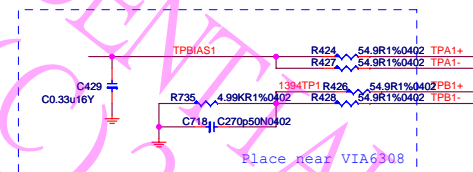
CLose to Connector



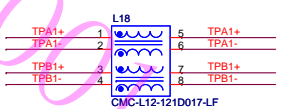
For Intel 1394 pinheader



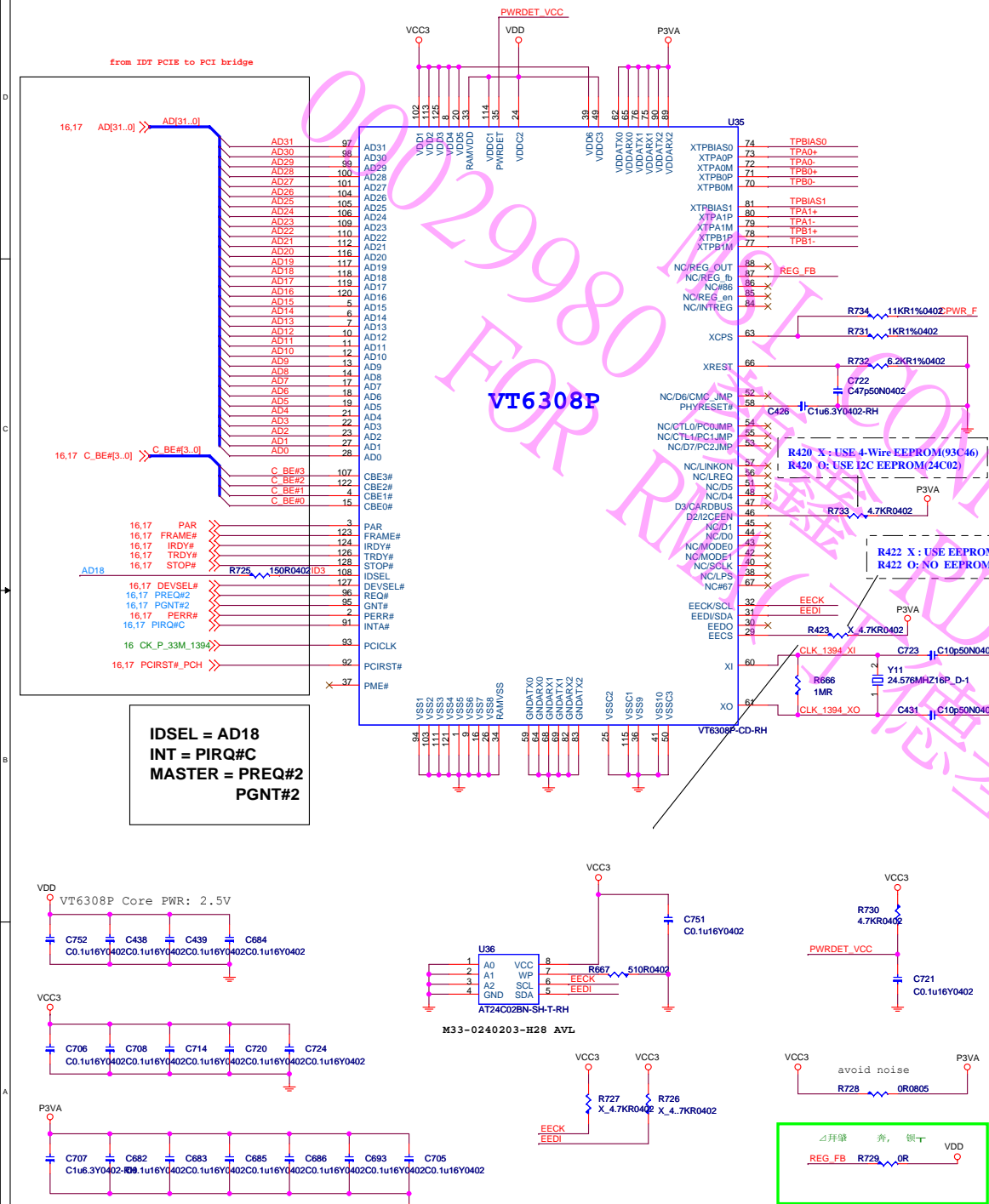
Front 1394 pin header



Close to Connector



100%



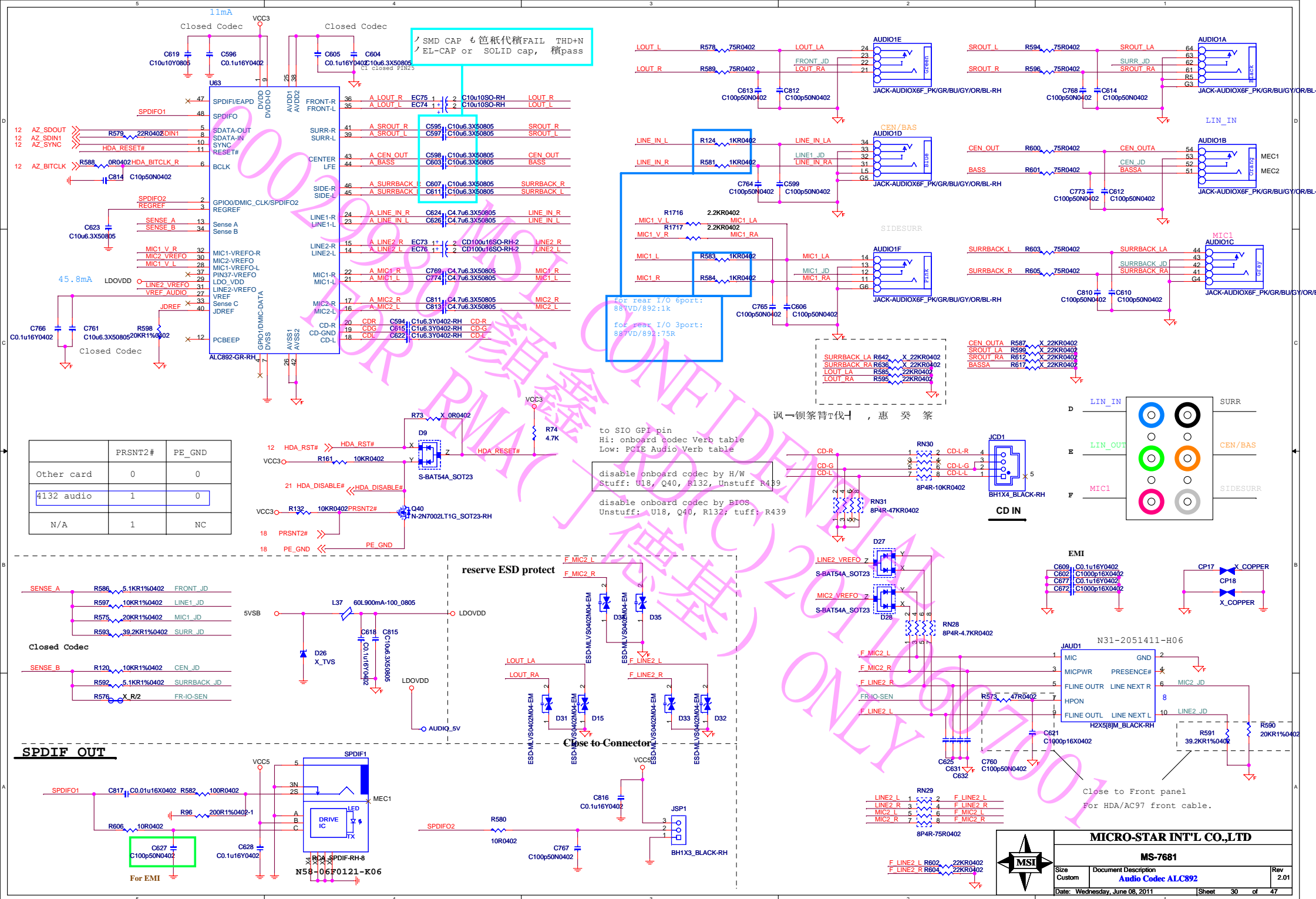
**MICRO-STAR INT'L CO.,LTD**

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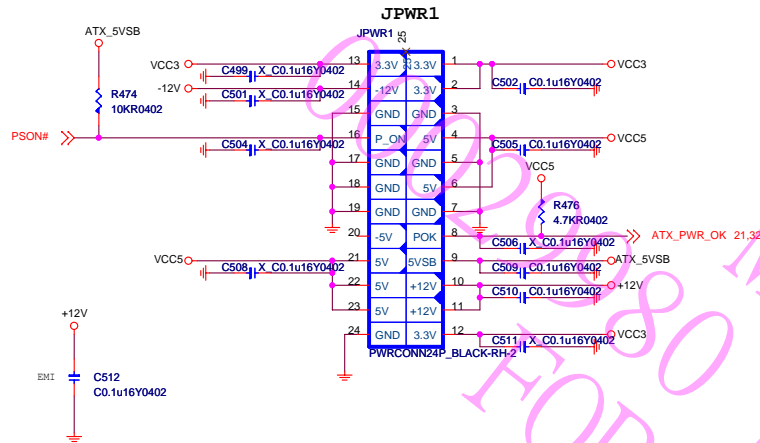
Size Custom	Document Description <b>VT6308P-1394</b>
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Rev	2.01
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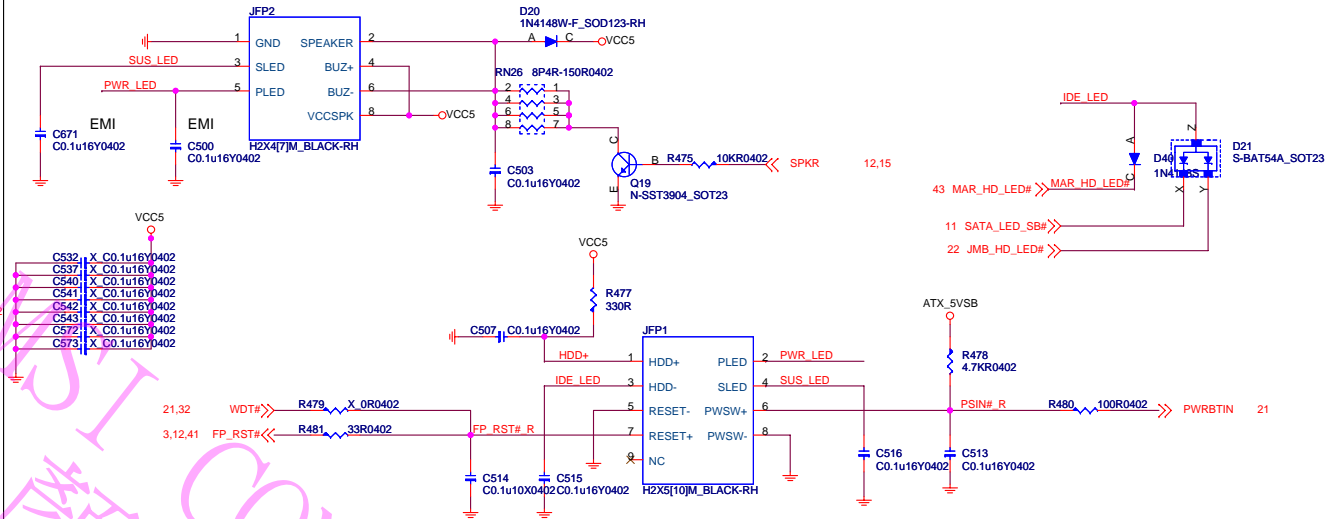
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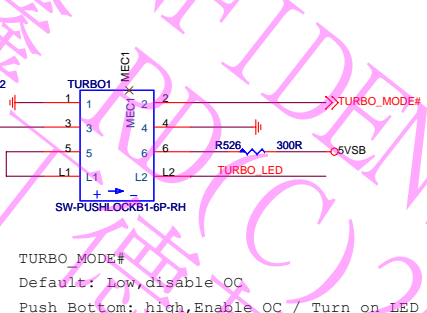
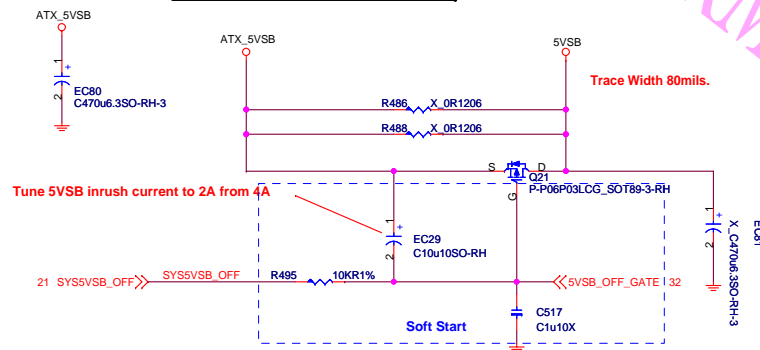
## ATX POWER CONNECTOR



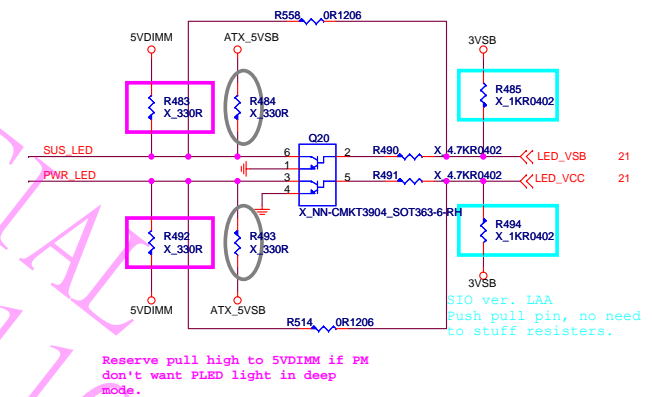
## FRONT PANNEL



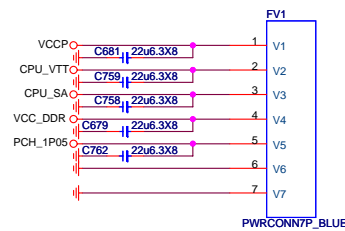
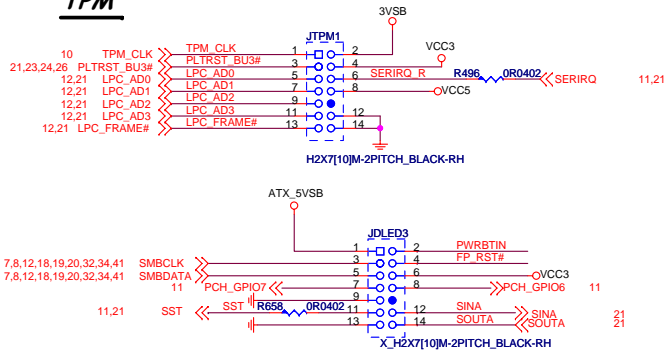
## 5VSB Power Switch



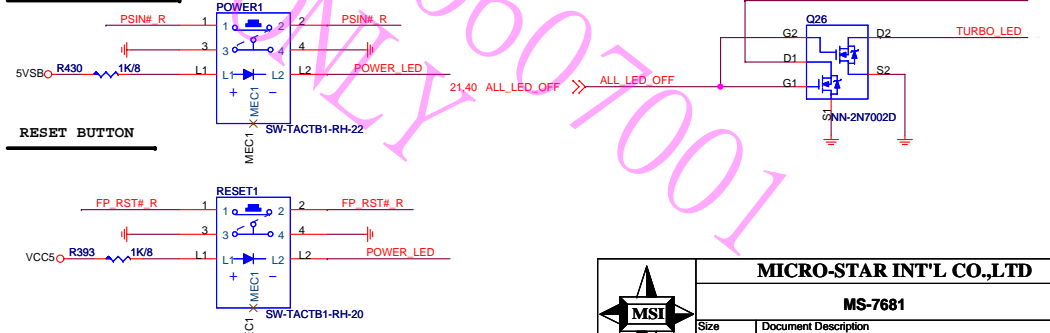
## LED ( for Fintek 71889)



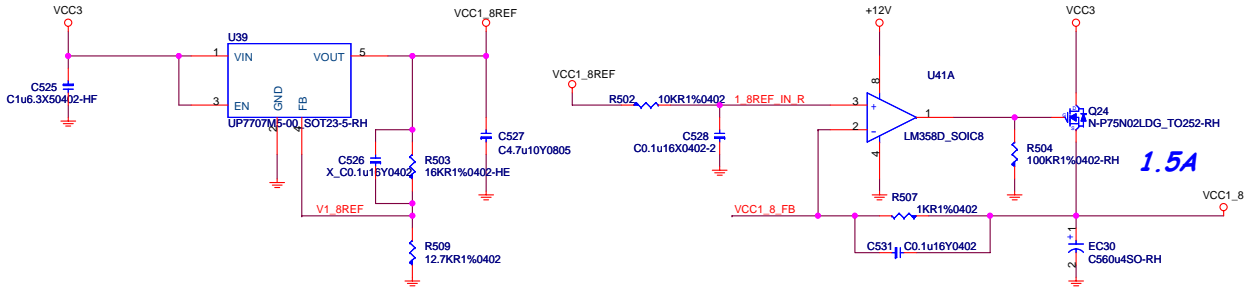
## TPM



## POWER ON BUTTON



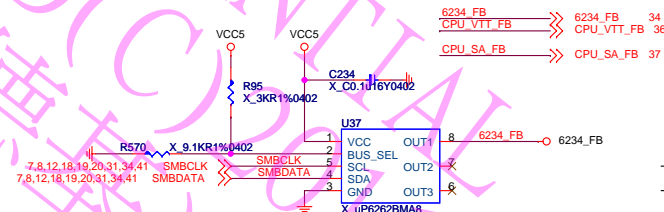
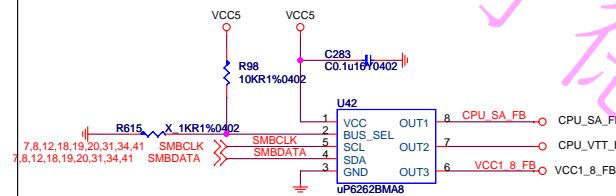
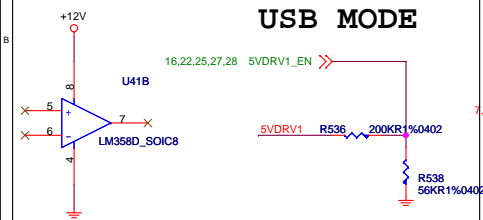
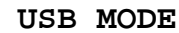
**VCC1\_8REF**



### 3VSB

[illegible]

### 3VSB

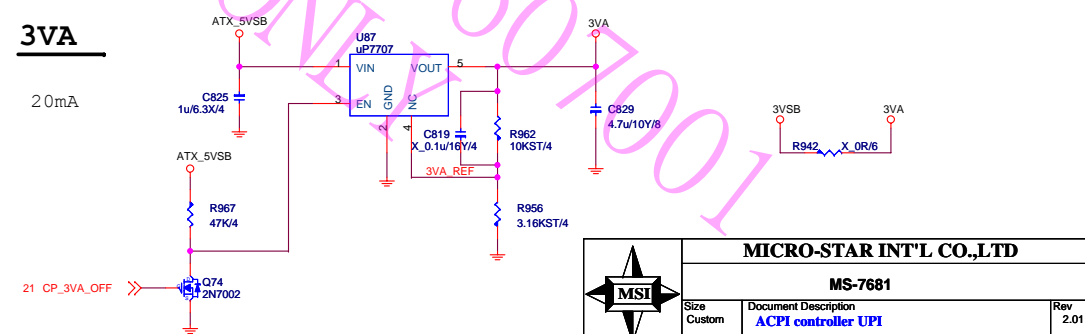


0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

**3VA**

The schematic shows three main power supply rails: VCC5, VCC3, and CHIP\_PWDG. VCC5 is connected to pin EC36 (C470u6.3SO-RH-3) through a resistor R281. VCC3 is connected to pin X\_10KR1%0402 (R535) and pin X\_20KR390402 (R534). The CHIP\_PWDG pin is connected to pin X\_N-MMBT3904\_NL\_SOT23 (Q30) through a resistor R537. A capacitor C470u6.3SO-RH-3 is connected between VCC5 and ground. A diode D470V100M0402 is connected between VCC3 and ground. A diode D470V100M0402 is connected between VCC3 and ground. A diode D470V100M0402 is connected between VCC3 and ground.

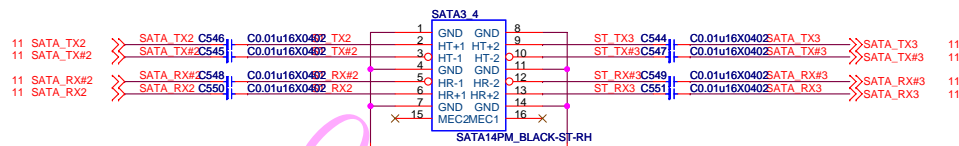


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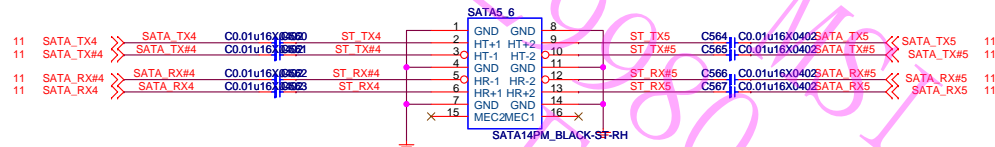
**MS-7681**

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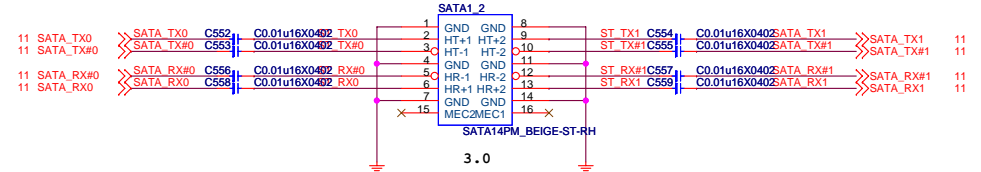
## SATA3-4



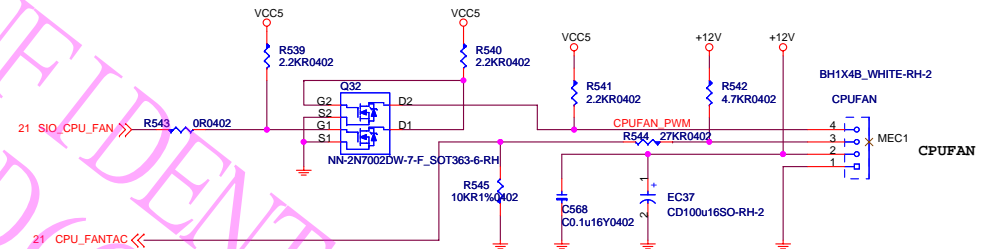
## SATA5-6



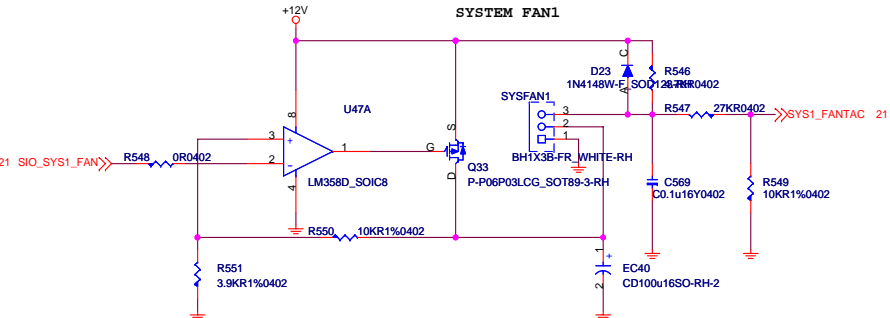
## SATA1-2



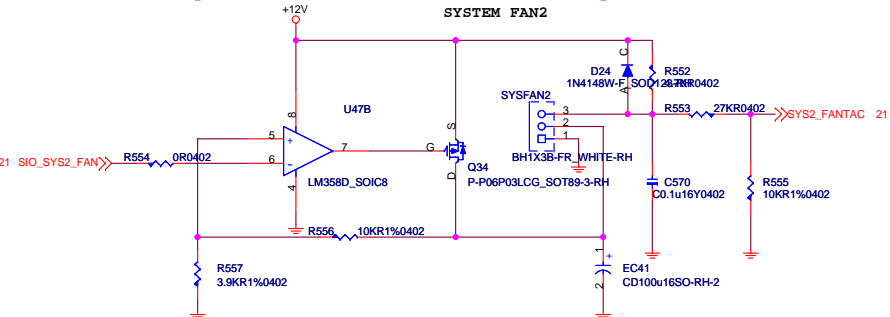
## CPU FAN-COUNTROL CIRCUIT



## SYSTEM FAN1



## SYSTEM FAN2

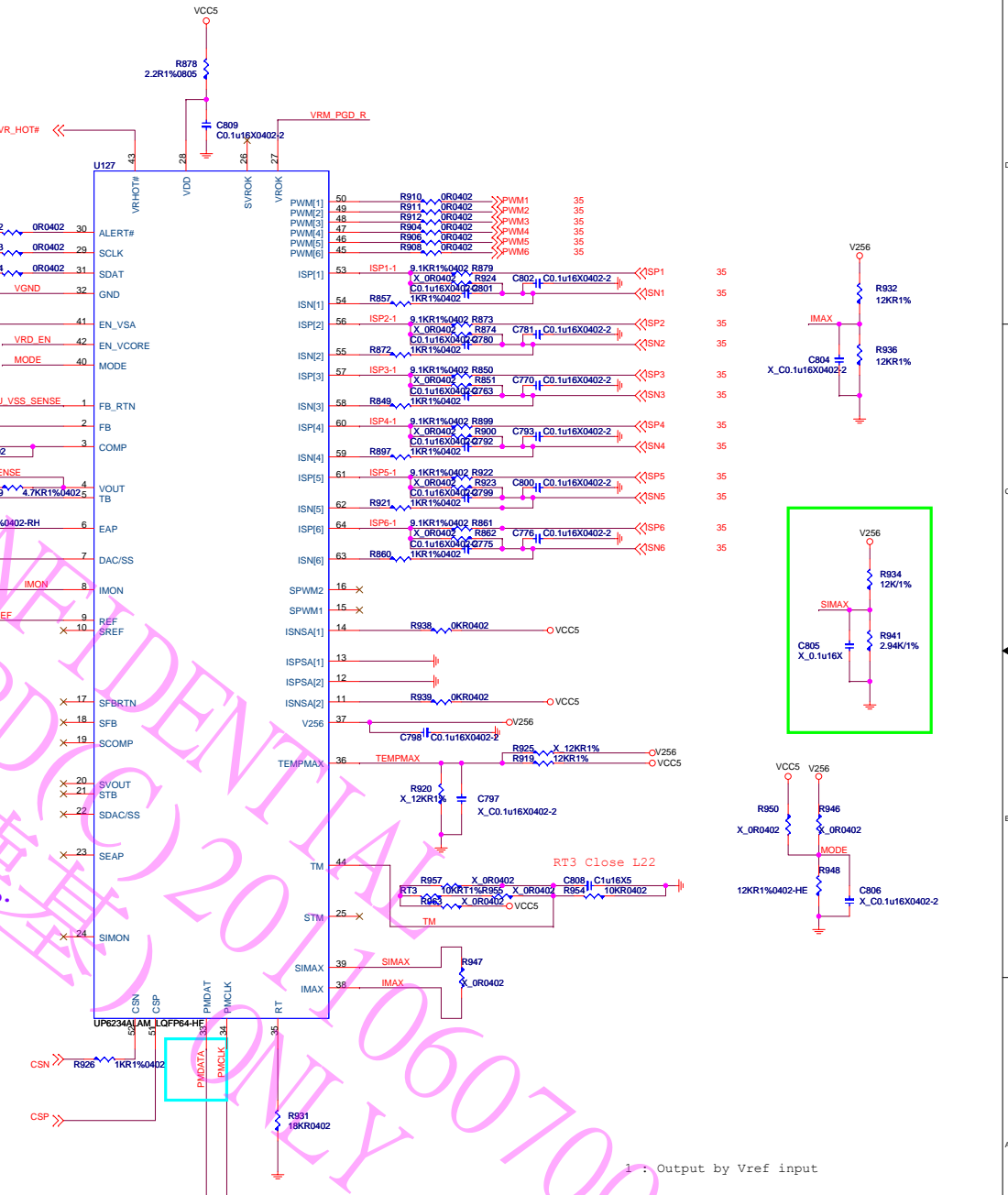
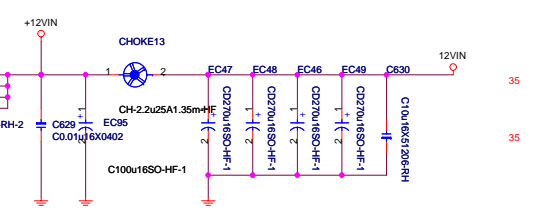
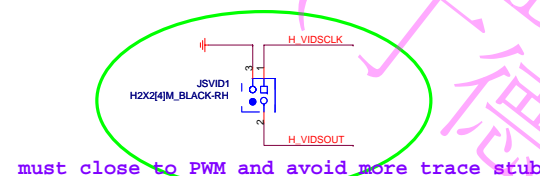
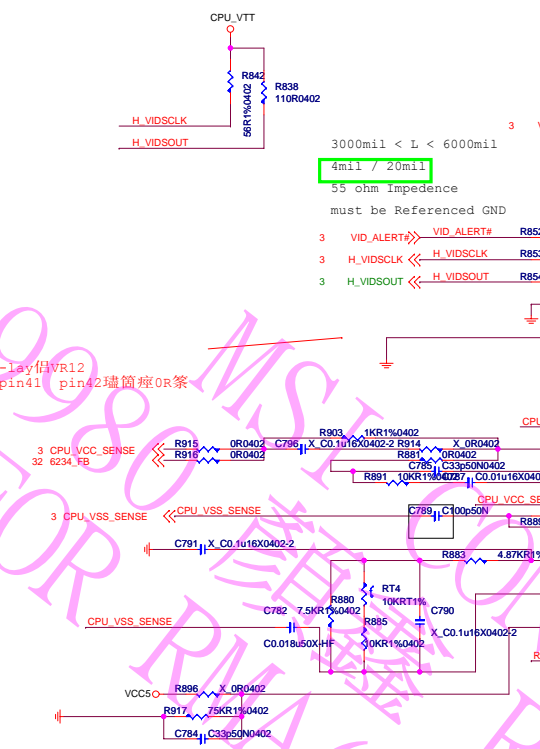
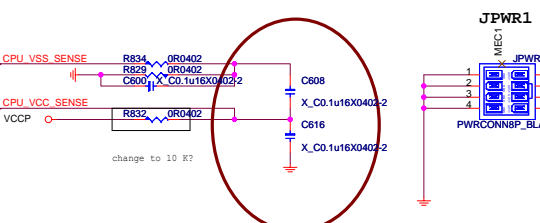
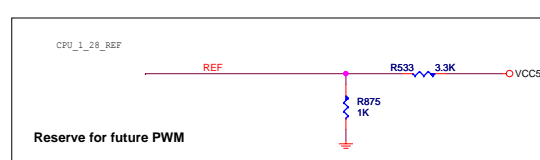
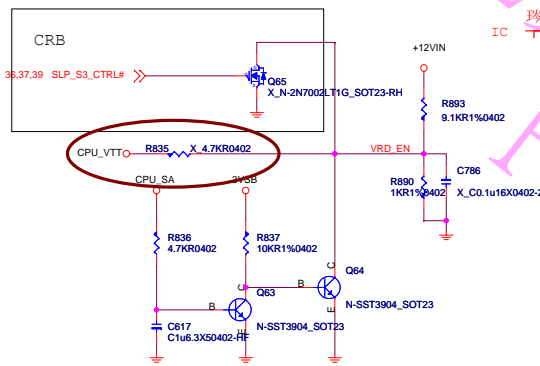


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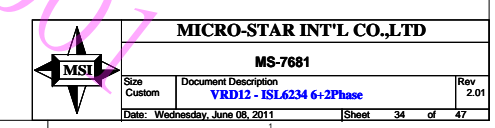
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[illegible]

1 : Output by Vref input



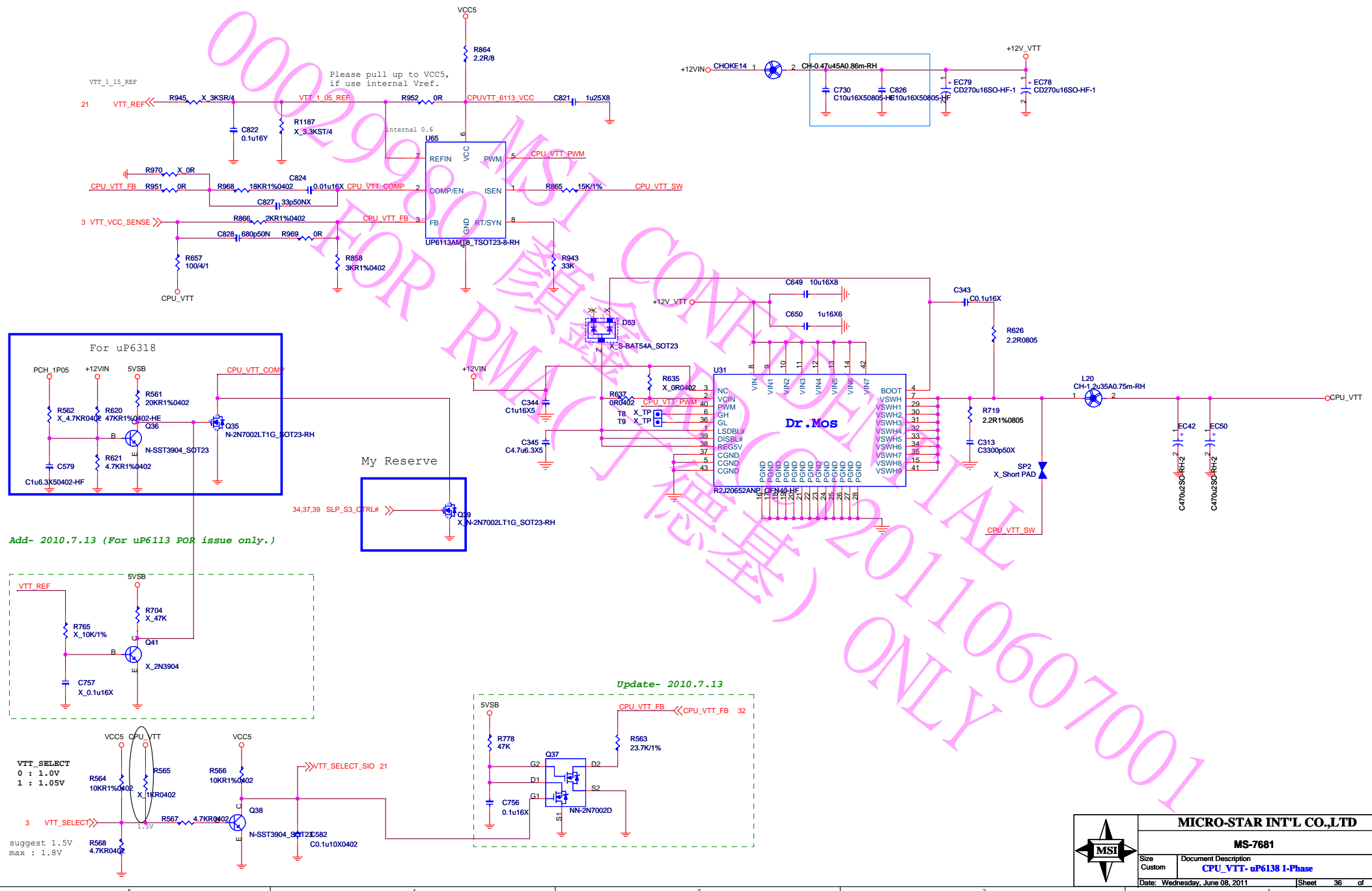


CPU\_VTT:1.05/1.00

CPU VTT 8.2A

$\text{Ripple} = 1.9(\text{vtt}) + 1.8(\text{sa})$

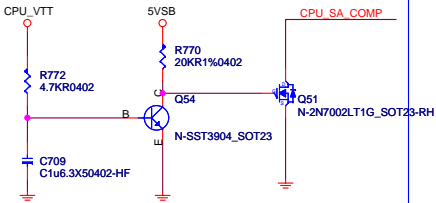
$5 \times 2 = 10\text{A} > 3.8\text{A}$



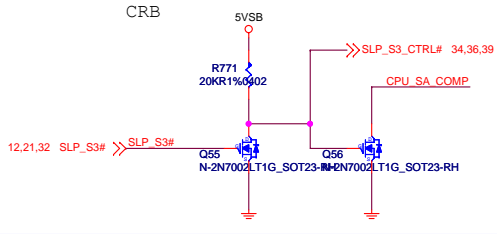
# CPU\_SA:0.925/0.85

SA Core =8.8A

Waiting CPU\_VTT Ready

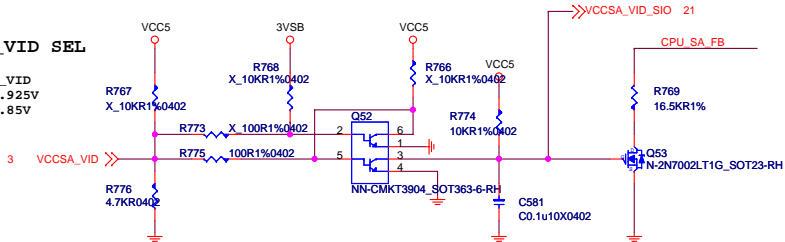


meet POFV Sequence



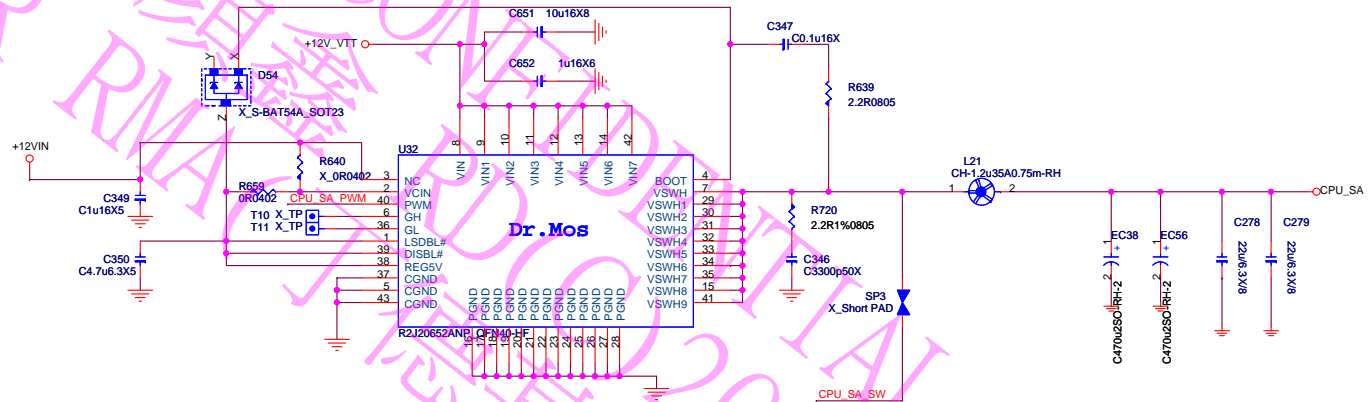
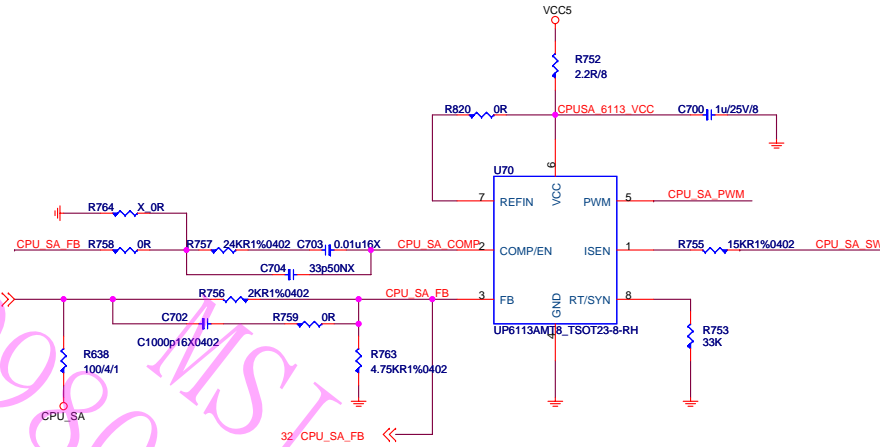
VCCSA\_VID SEL

VCCSA\_VID  
0 : 0.925V  
1 : 0.85V



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.85V
High	0.925V



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Size: Custom

Document Description: CPU\_SA-uP6113-1Dr.MOS

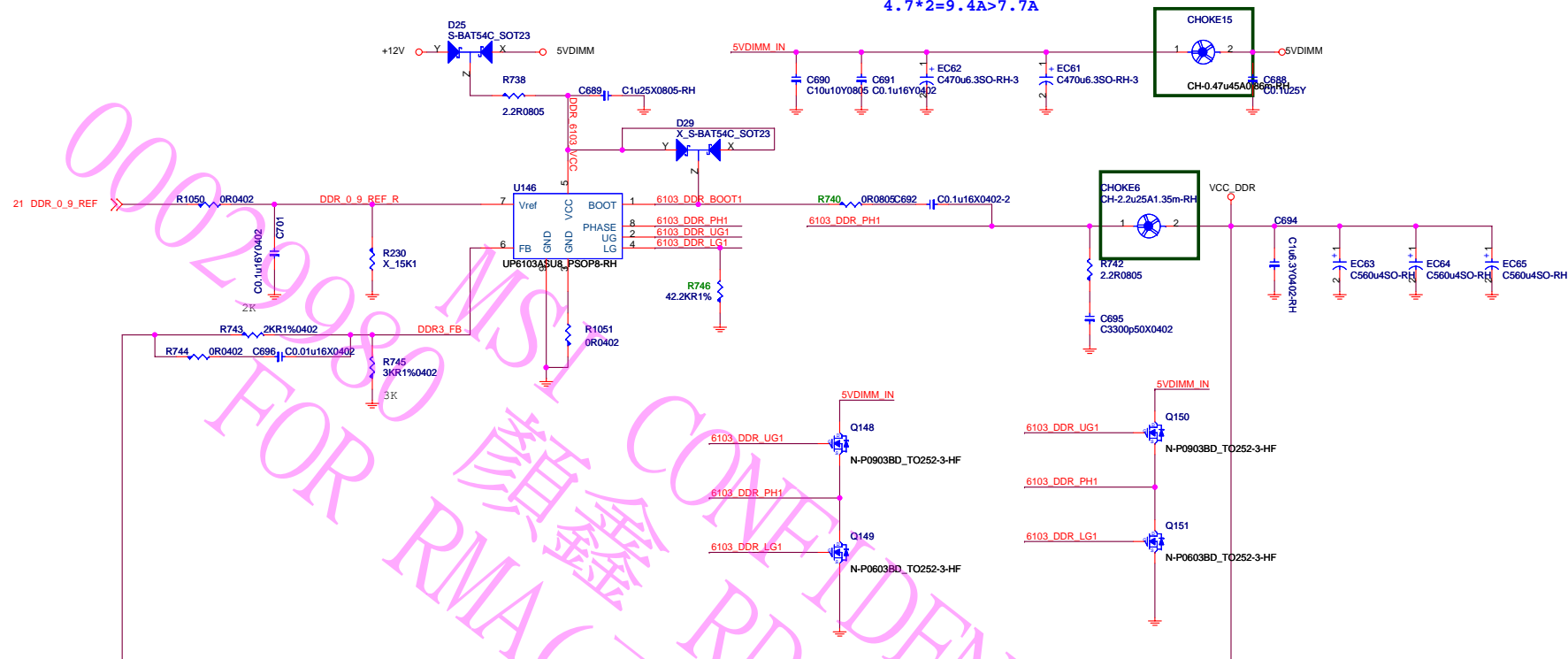
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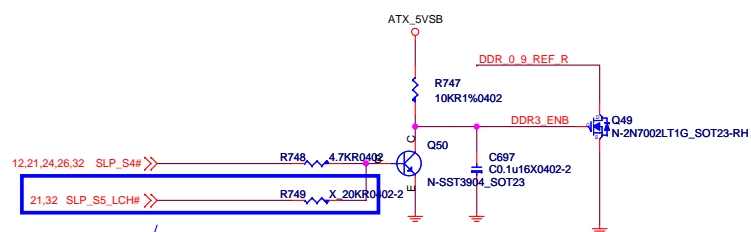
4.5A FOR CPU  
15A FOR 4DIMM  
1A FOR DDR VTT

$I_{ripple} = 7.7A$   
 $4.7 * 2 = 9.4A > 7.7A$



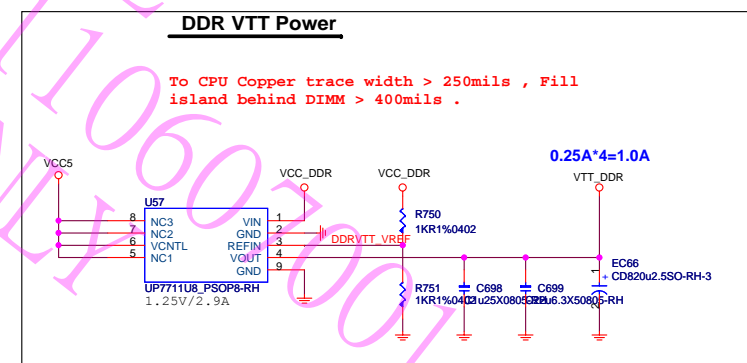
VTT\_DDR

VTTDDR 0V75



## Meet Intel Power Down Sequence

If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#,else use SLP\_S4#.



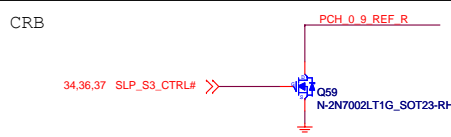
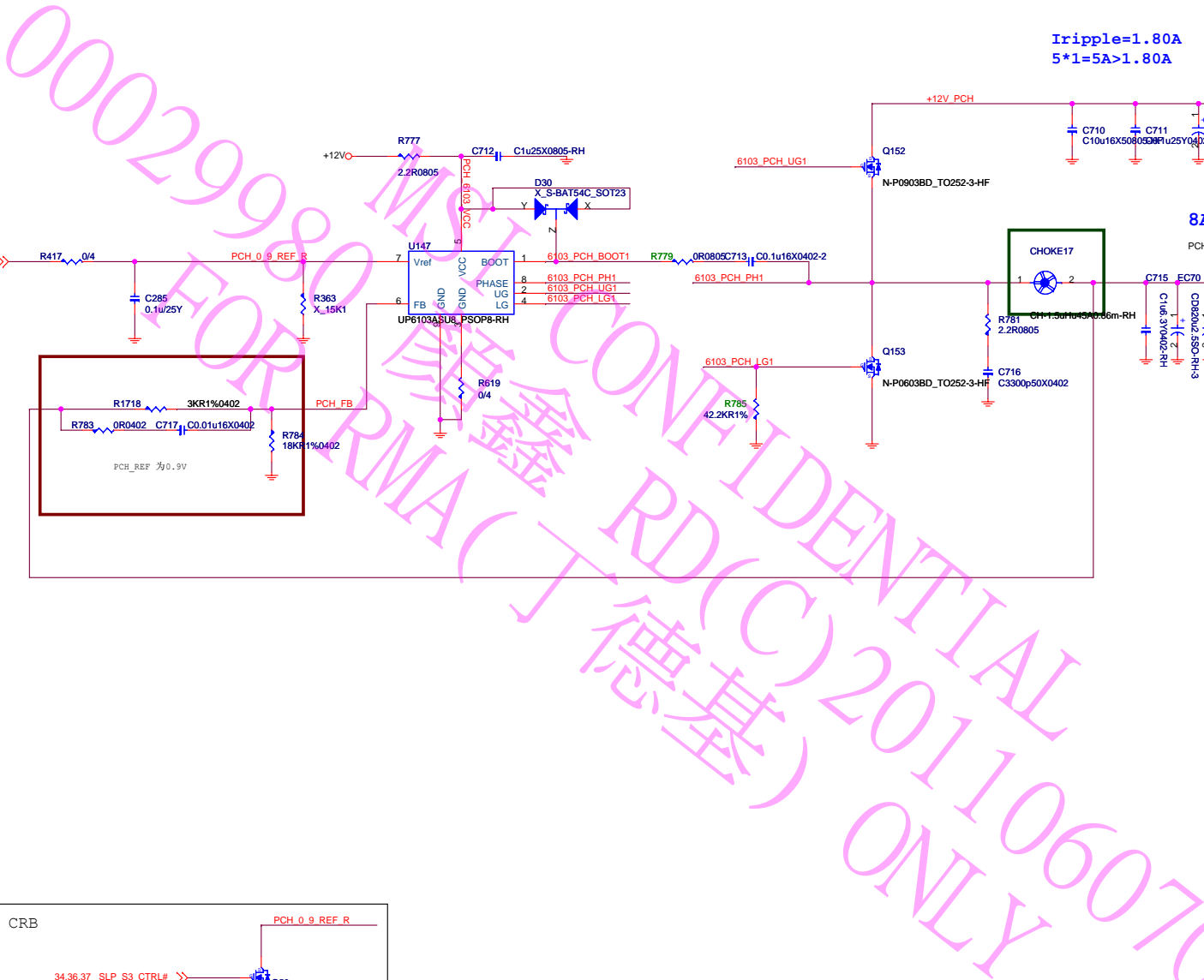
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	uP6103A	uP6138
PIN1	BOOT	BOOT
PIN2	UG	UG
PIN3	GND	VREFIN
PIN4	LG	LG
PIN5	VCC	VCC
PIN6	FB	FB
PIN7	Vref	OCP/EN
PIN8	PHASE	PHASE
PIN9	GND	GND

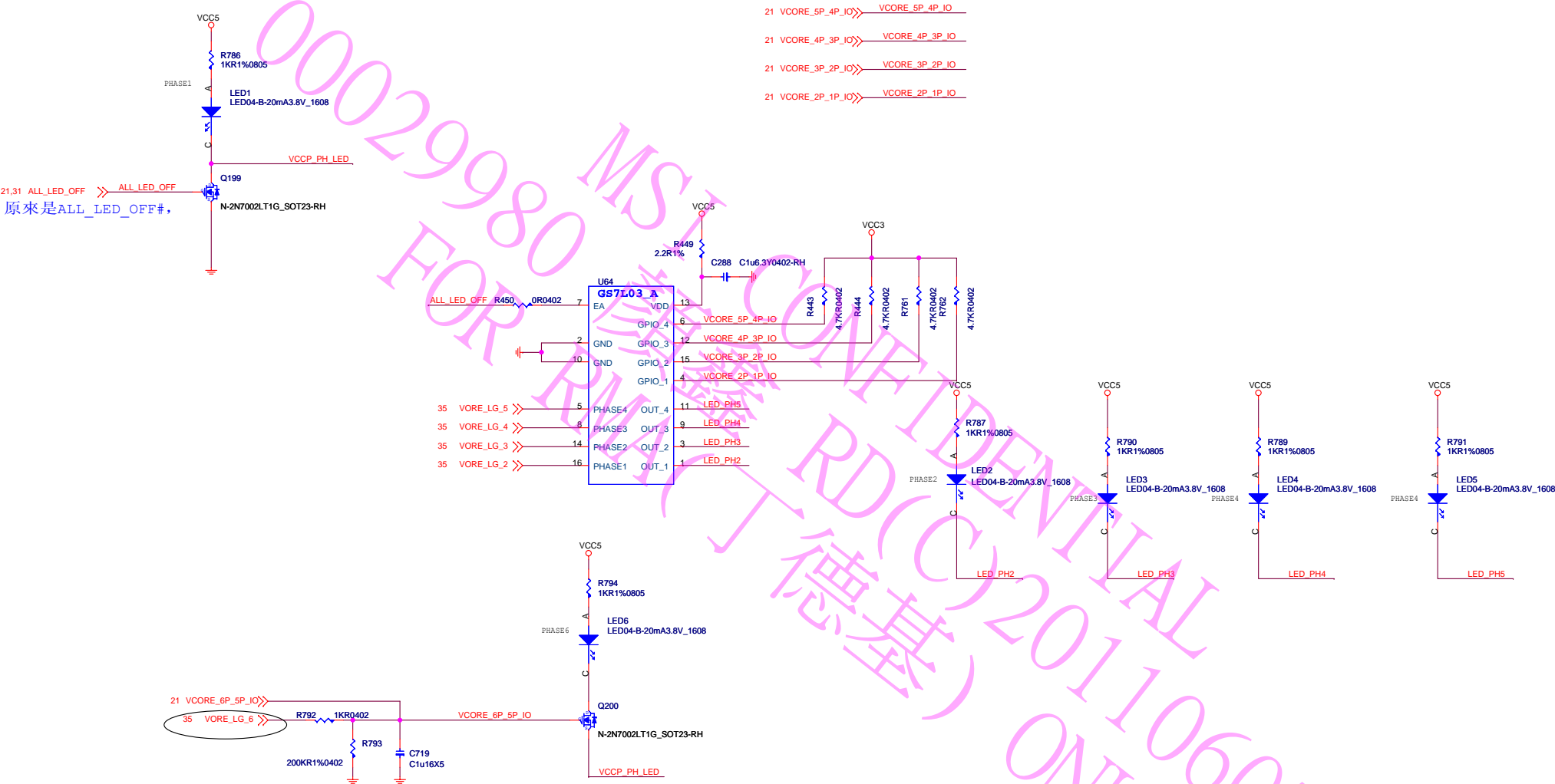


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all on board LED switch



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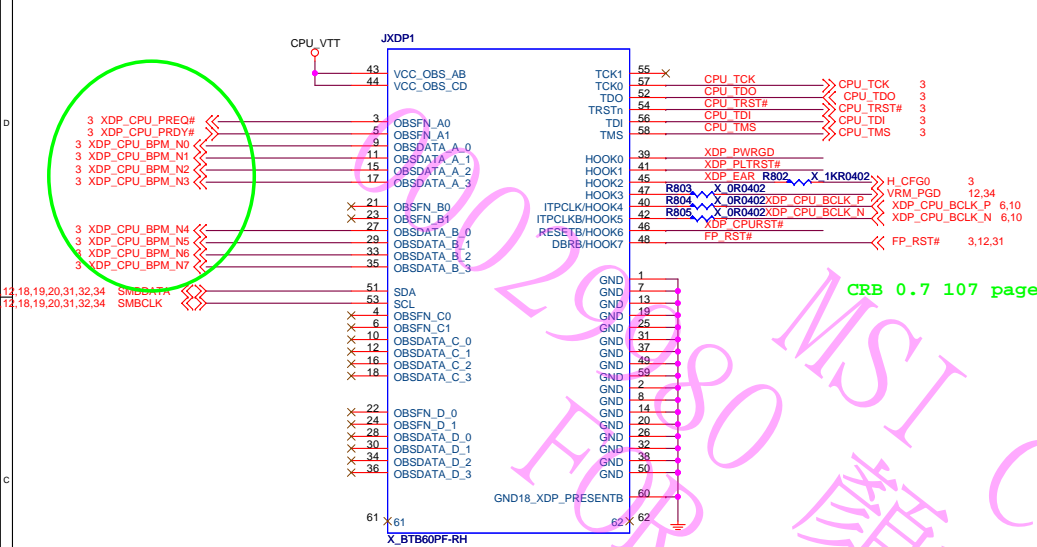
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## Reserve debug port 5020

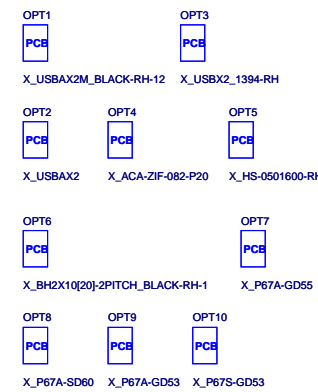
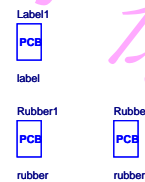
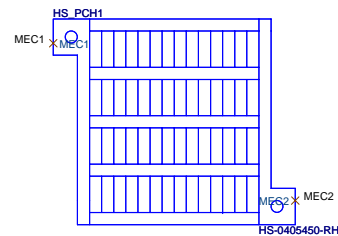
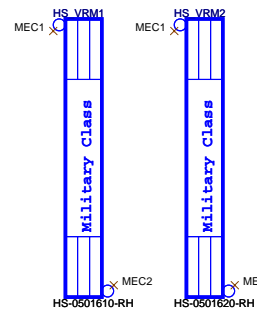
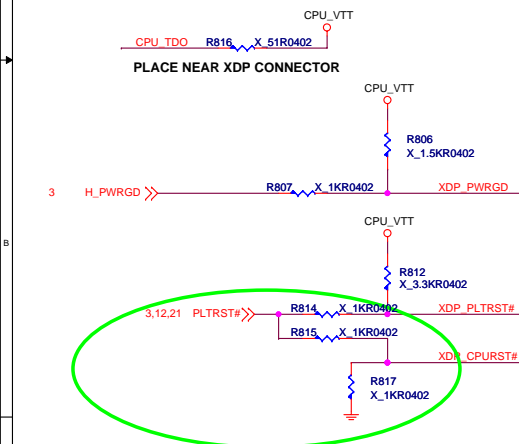
## PCH XDP

## 瘡代謎

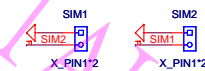


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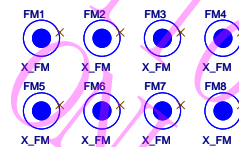
## PCH XDP PWRGD/RESET



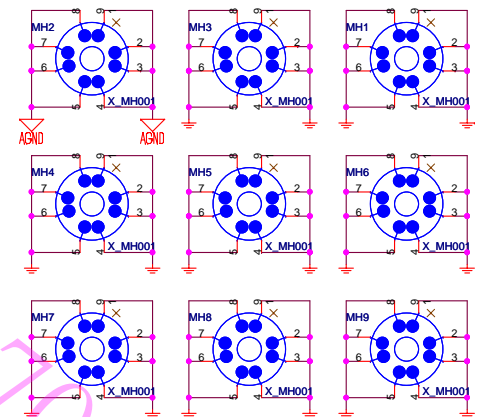
## Simulation



## Optical Fiducial Marks-120



## Optical Fiducial Marks-100



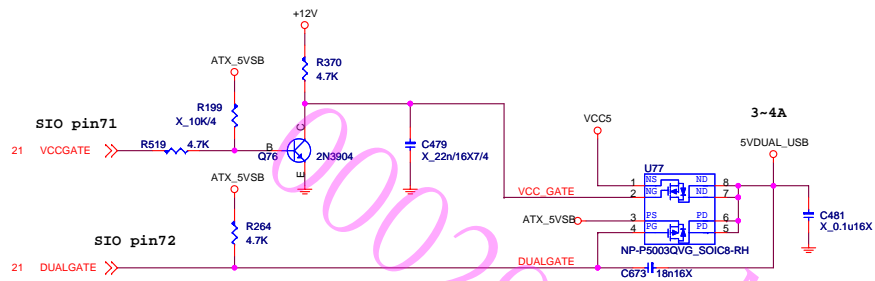
## Mounting Holes

MICRO-STAR INT'L CO.,LTD			
MS-7681			
Size	Document Description	Rev	
Custom	XDP / Manual Parts	2.01	
Date:	Wednesday, June 08, 2011	Sheet	41 of 47

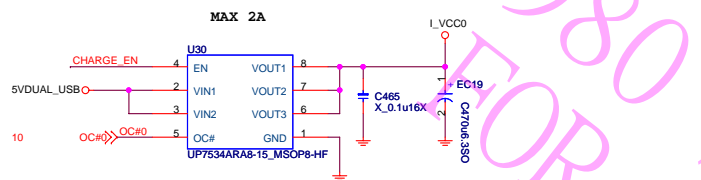
PD0-0758111-E48, 腳  
PD0-0758111-G37, 腳

吹邻紅 (MSIS)  
吹邻紅 (MSIS)

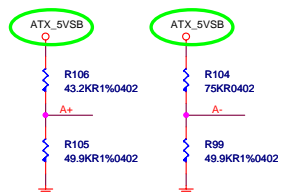
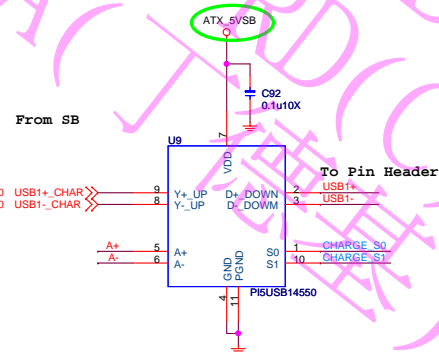
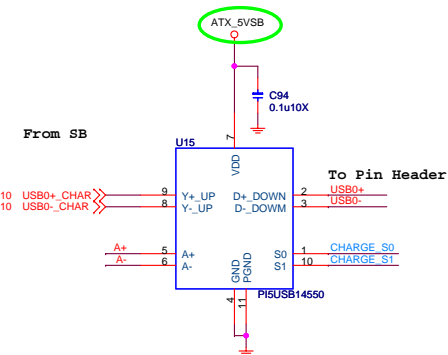
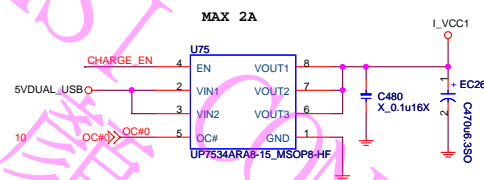
## 5VDUAL\_USB



## USB POWER FOR PORT 0 for Battery Charging



## USB POWER FOR PORT 1 for I charge



A type  
2.70V< D+ <3.1 V  
1.85V< D- < 2.1V  
For i-Pad / i-Phone 4G charges current up to 1.6A.

SIO GPIO40 Pin7 (VBAT for New F71889AD)

USB\_CHARGE:

0: Don't support USB charge and resume.  
1: Support USB charge and resume.

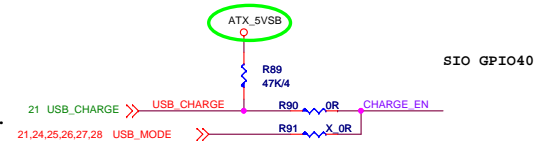
1st boot , H/W default support USB charge.

SIO GPIO50 (I\_VSB3V)

BC\_SEL: (PUSH PULL)

0: Support DCP device(don't support usb link and resume)  
1: Support CDP (Support usb link and resume)

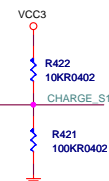
1st boot , H/W default support DCP.



SIO GPIO50

21 CHARGE\_S1

Pin power I\_3VSB  
Register power I\_3VSB  
Register reset I\_3VSB



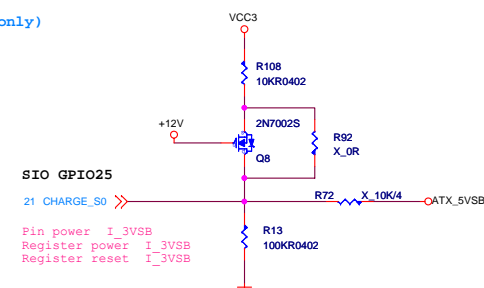
SIO GPIO25 (I\_VSB3V)

SIO GPIO50 (I\_VSB3V)

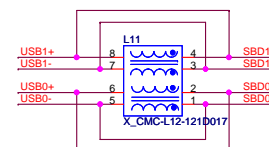
CHARGE\_S0: (PUSH PULL)

CHARGE\_S1: (Open Drain only)

S0	S1
AUTO:	0 0
DCP:	0 1
X:	1 0
Y:	1 1



## FRONT USB PORT 0,1



SIO GPIO pin 15

Default low

LOW= support I charge

1st boot H/W default support i charge

L\_VCC0

L\_VCC1

OC0

JUSB1

SBD0+

SBD0-

SBD1+

SBD1-

BH2X5[9]\_BLACK-RH-9

